



# Q57H-AD

V 10

## SCHEMATICS TABLE:

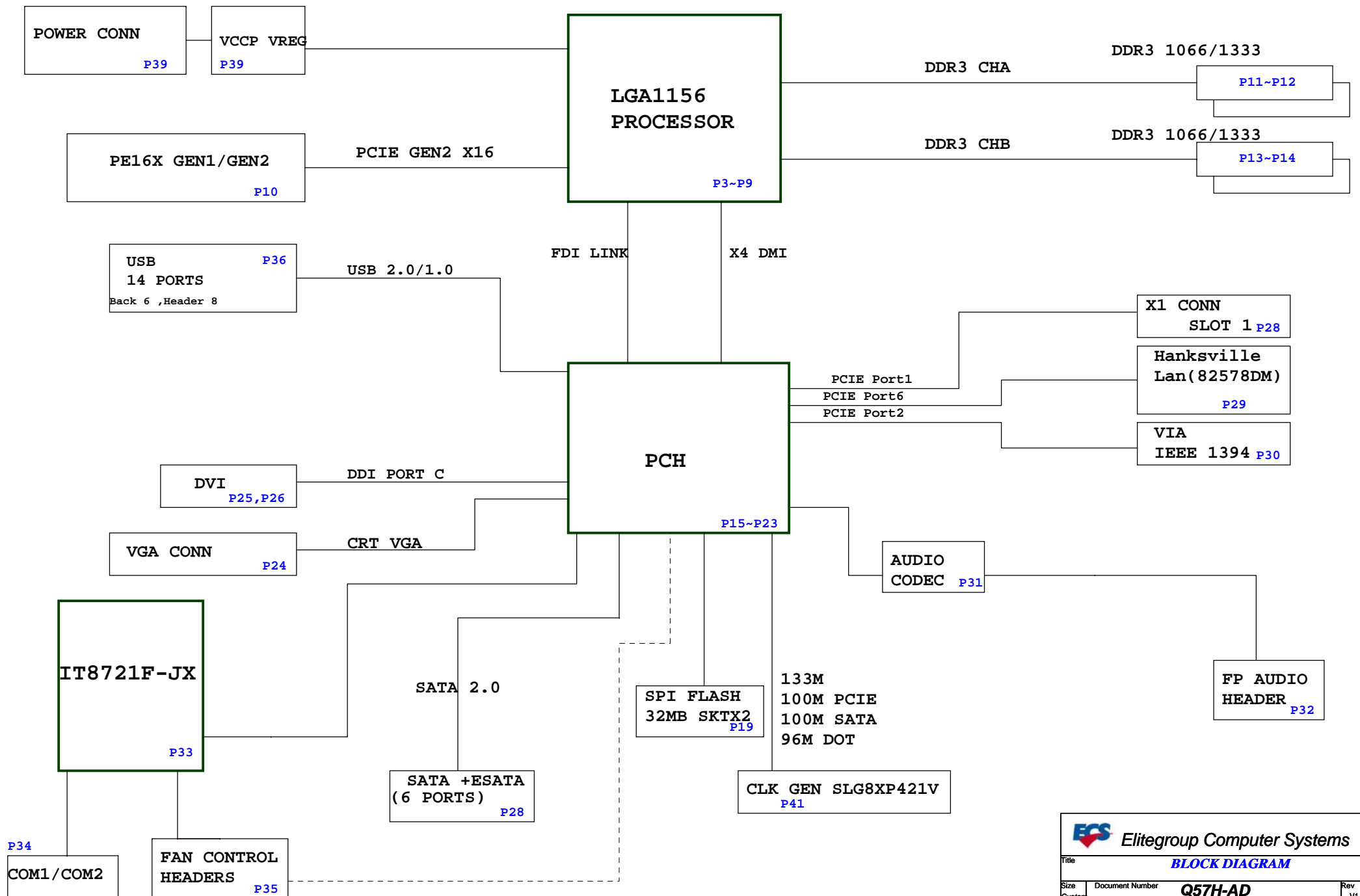
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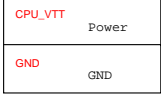
## REVISION HISTORY:

Rev	Date	Notes
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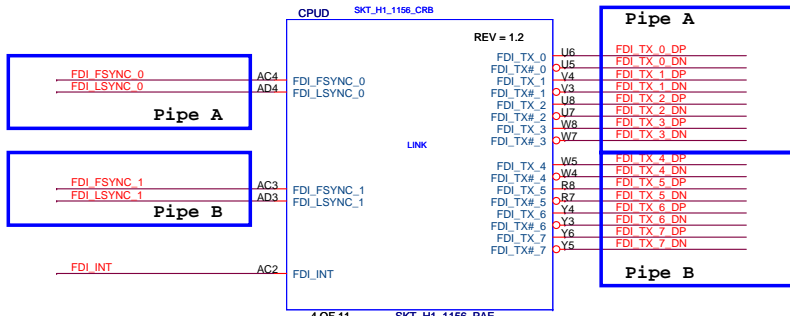
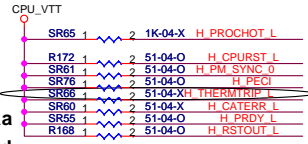
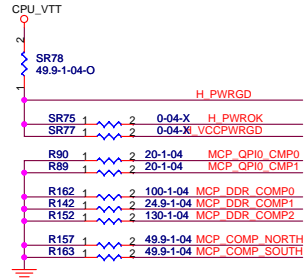
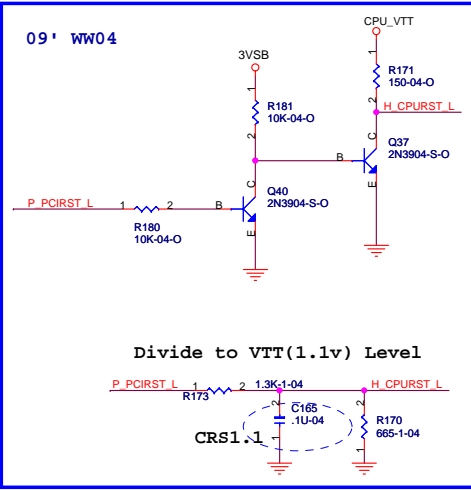
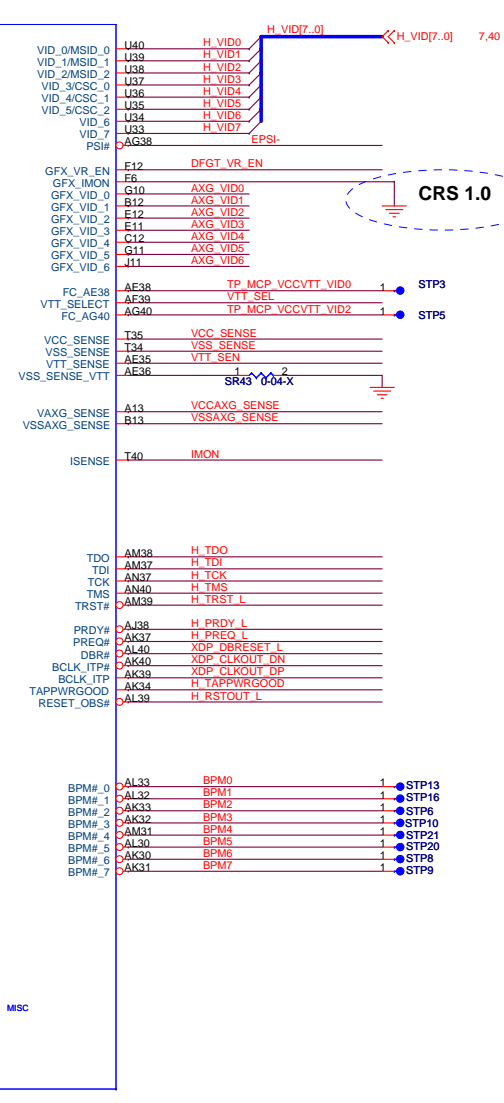
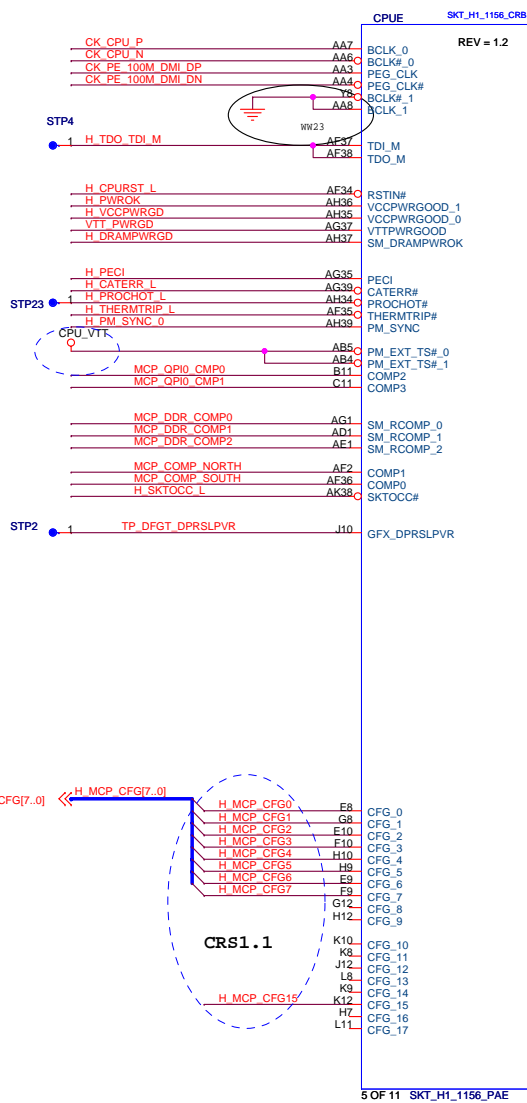
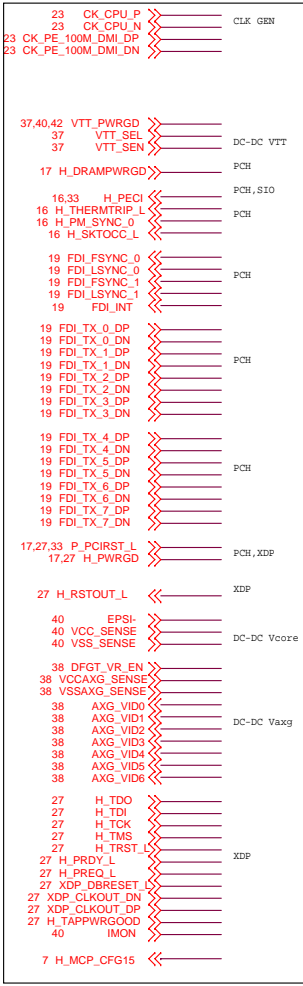
@ ECS  
CONFIDENTIAL @

Elitegroup Computer Systems			
Title <i>Cover Page</i>			
Size Custom	Document Number <b>Q57H-AD</b>	Rev V1.0	
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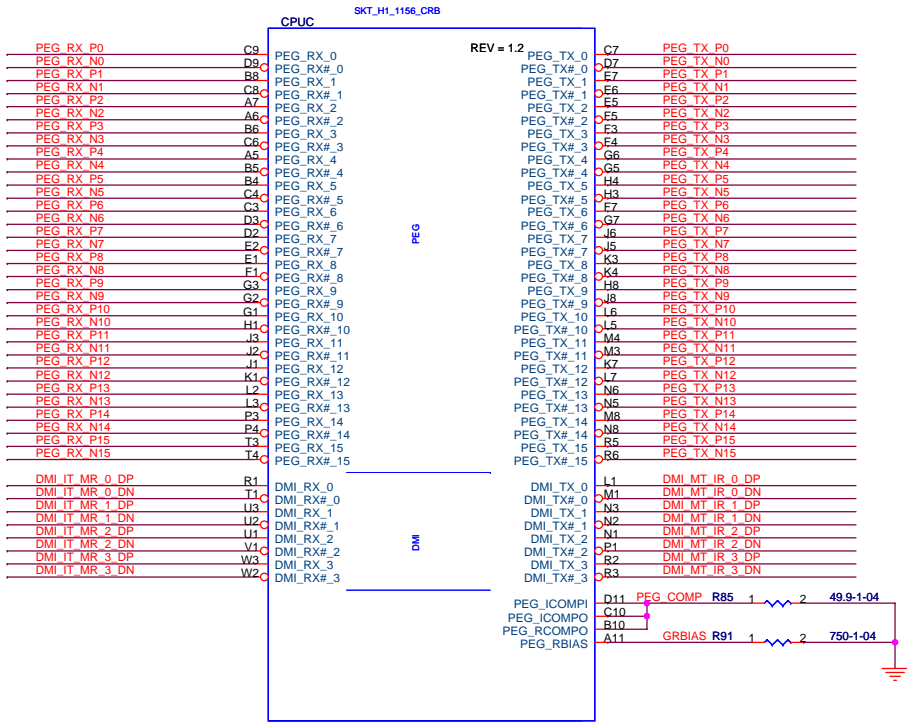
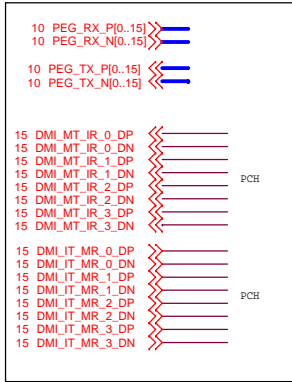
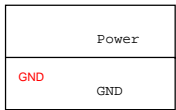




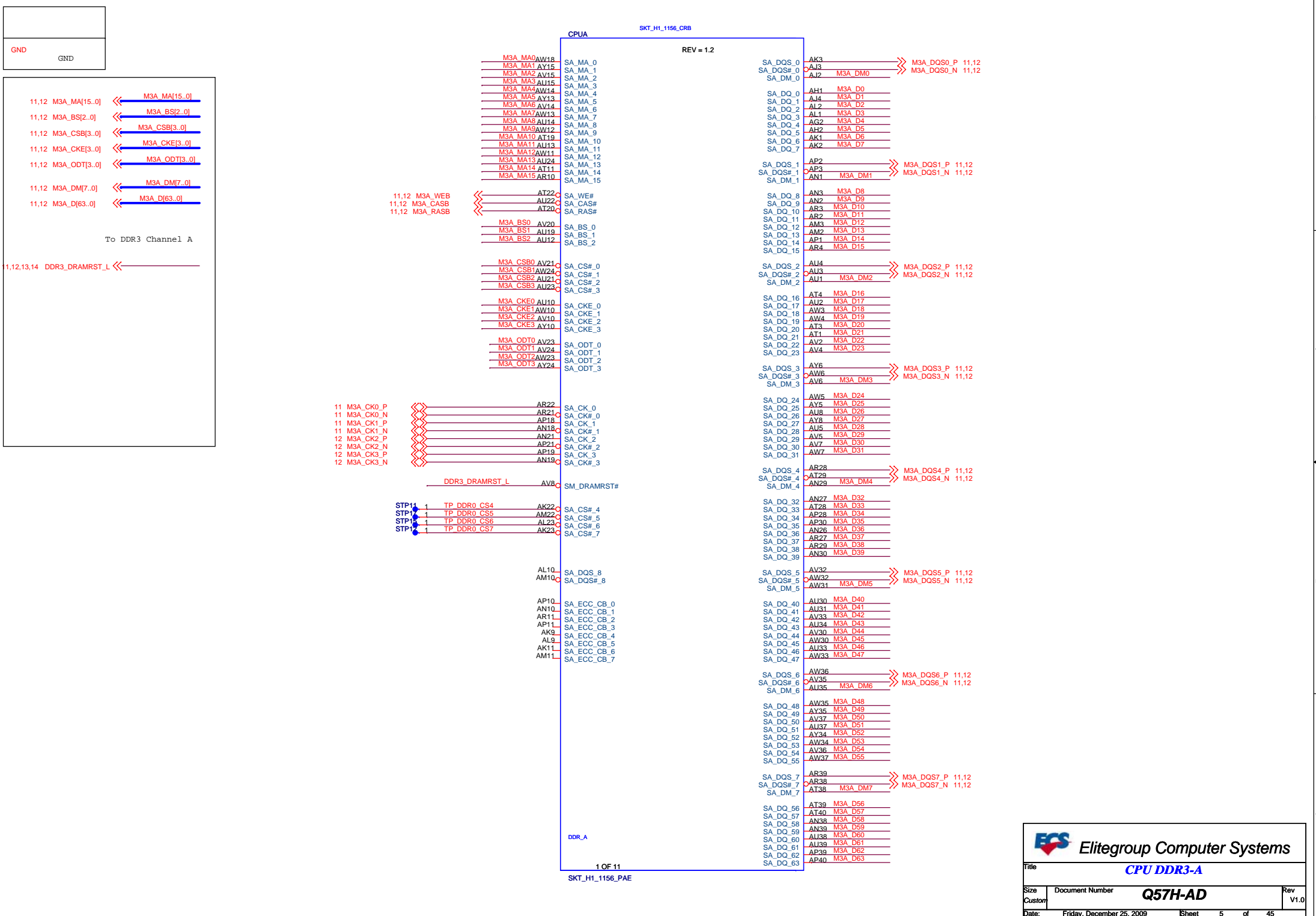
BCLK(133MHz) for CPU/MEM/GPU  
PEG\_CLK(100MHz) for PCIE/DMI/FDI



Ra for PRDY emptied

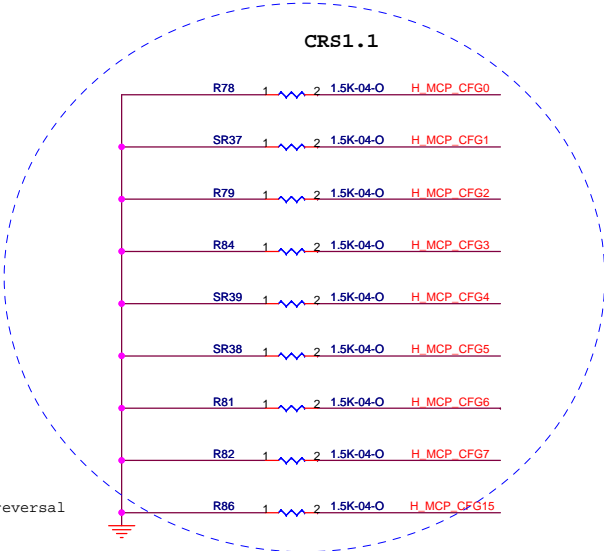
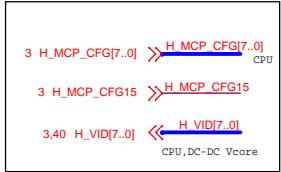


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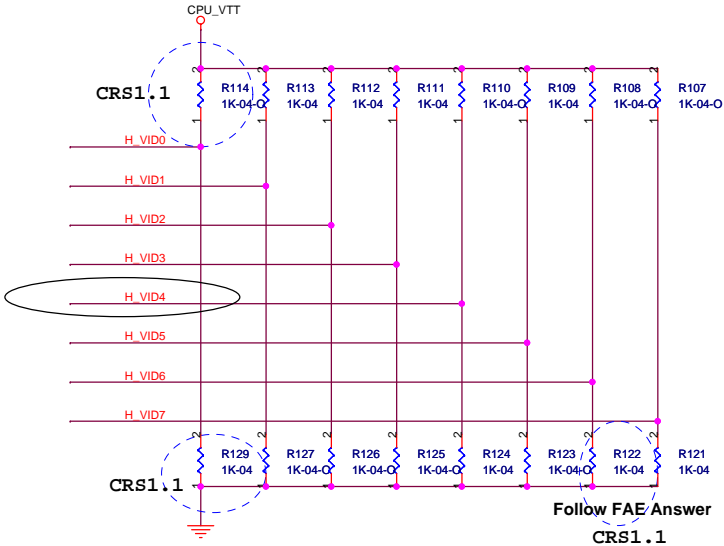


CPU_VTT	Power
GND	GND



CFG(1:0)  
Desktop  
11 PCIe16X  
10 PCIe18X  
CFG2,4,5,6,7~17  
Reserved configuration land  
CFG3  
Havendale PCIe static Lan Numbering reversal


CFG	Havendale	Lynnfield			
0	REVERSED	1	11=1*16X	0	10=2*8X
1	REVERSED	1		1	
2	REVERSED			REVERSED	
3	Static Lane Number Reversal			REVERSED	
4	REVERSED			REVERSED	
6	REVERSED				
7	REVERSED				
15	REVERSED				
0,1,2,3,4,5 ALL HAVE INTERNAL PULL-UPS					



POWER ON CONFIGURATION (POC)TABLE

	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG CSC0	1	lcc(MAX)=120A	lcc(MAX)=120A
VID4	IMON CONFIG CSC1	0		
VID5	IMON CONFIG CSC2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

\*MSID(2:0)  
110 Lynnfield and Havendale support  
\*CSC(0:2)  
Iout Gain and POC setting  
100 ICC(max) 80A~100A  
101 ICC(max) 100A~120A  
110 ICC(max) 120A~140A



Elitegroup Computer Systems

Title

CPU CFG

Size

Document Number

Q57H-AD

Rev

V1.0

Date:

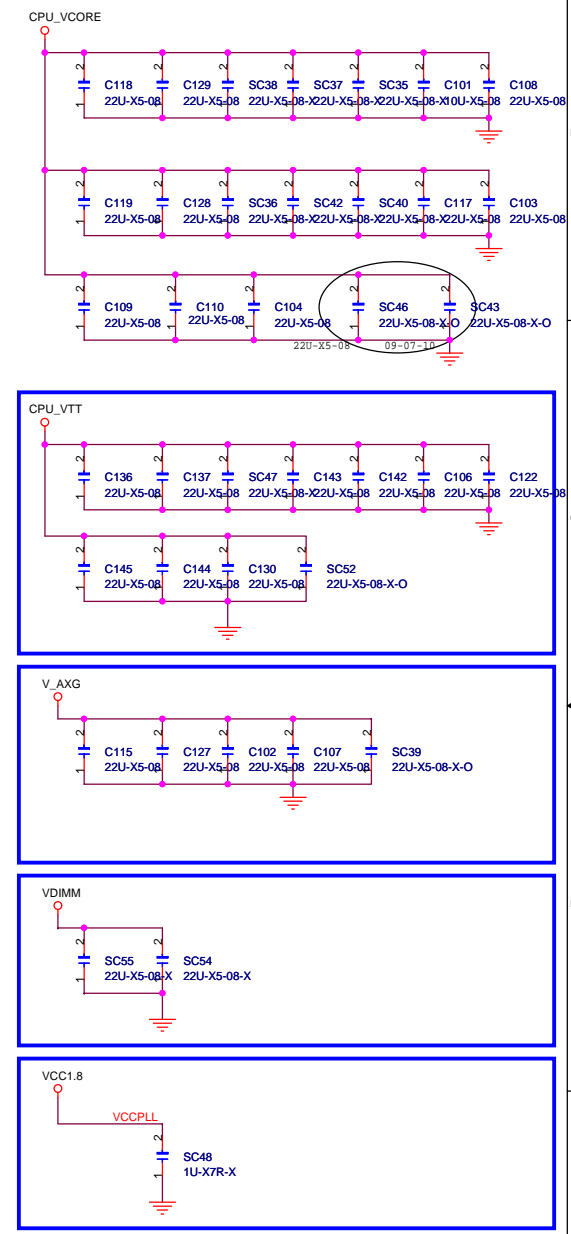
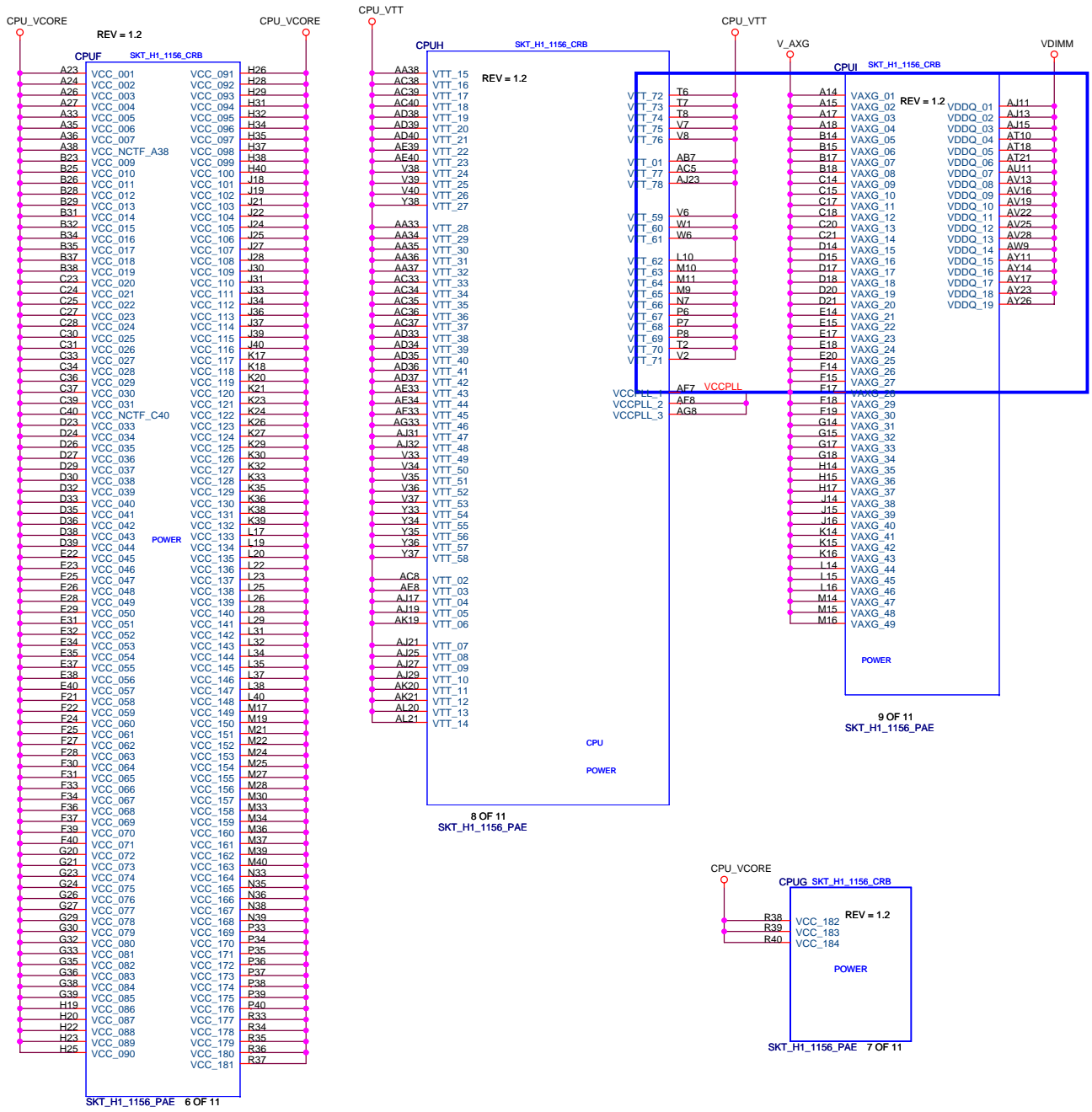
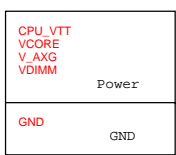
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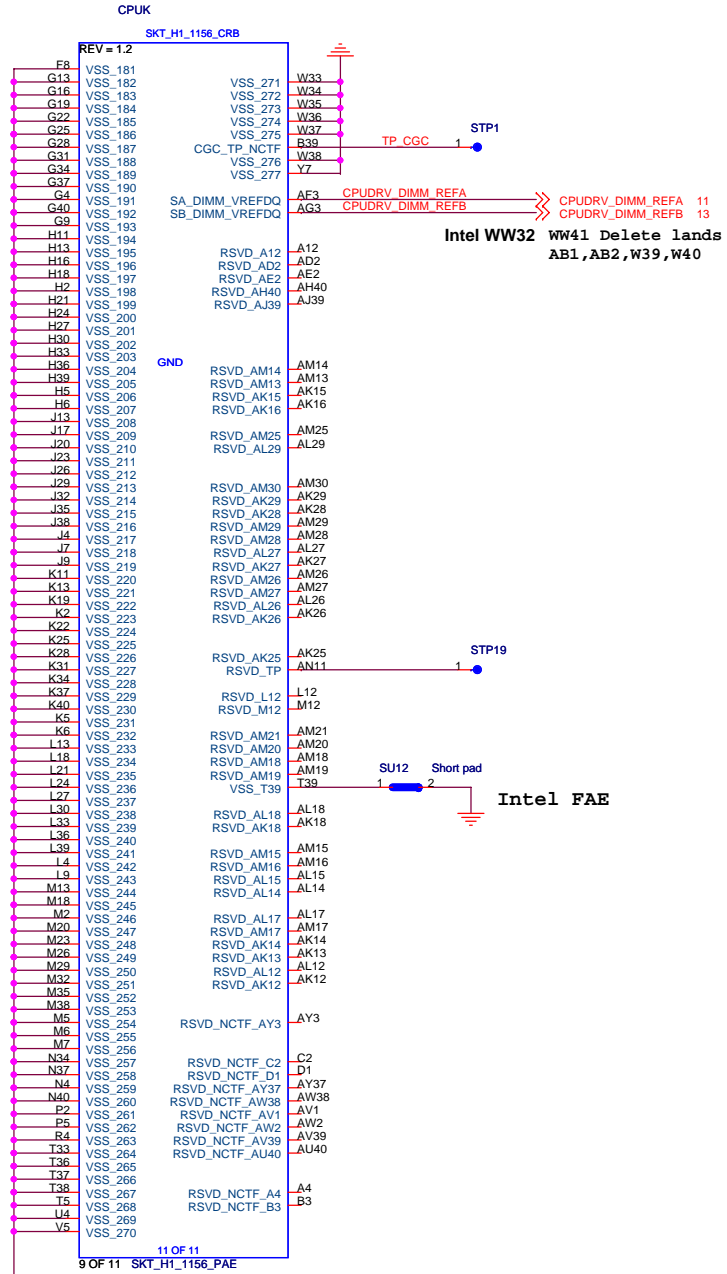
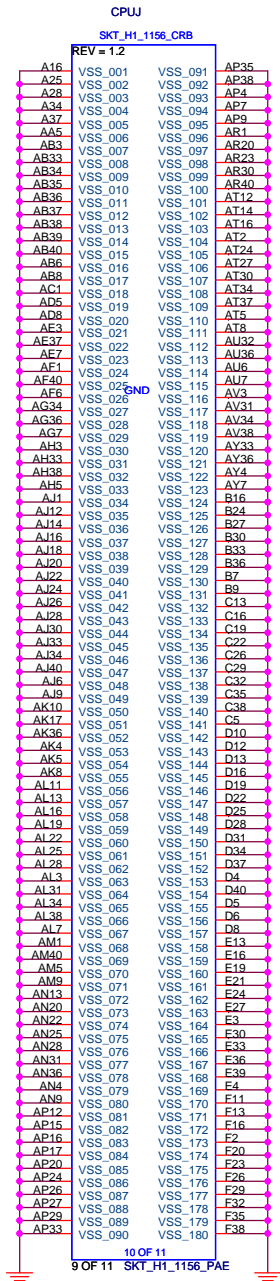
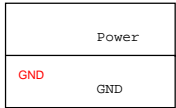
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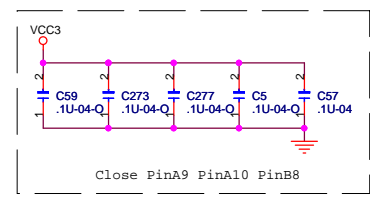
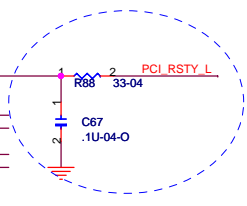
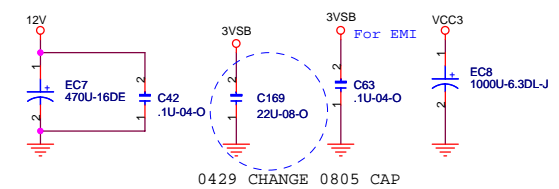
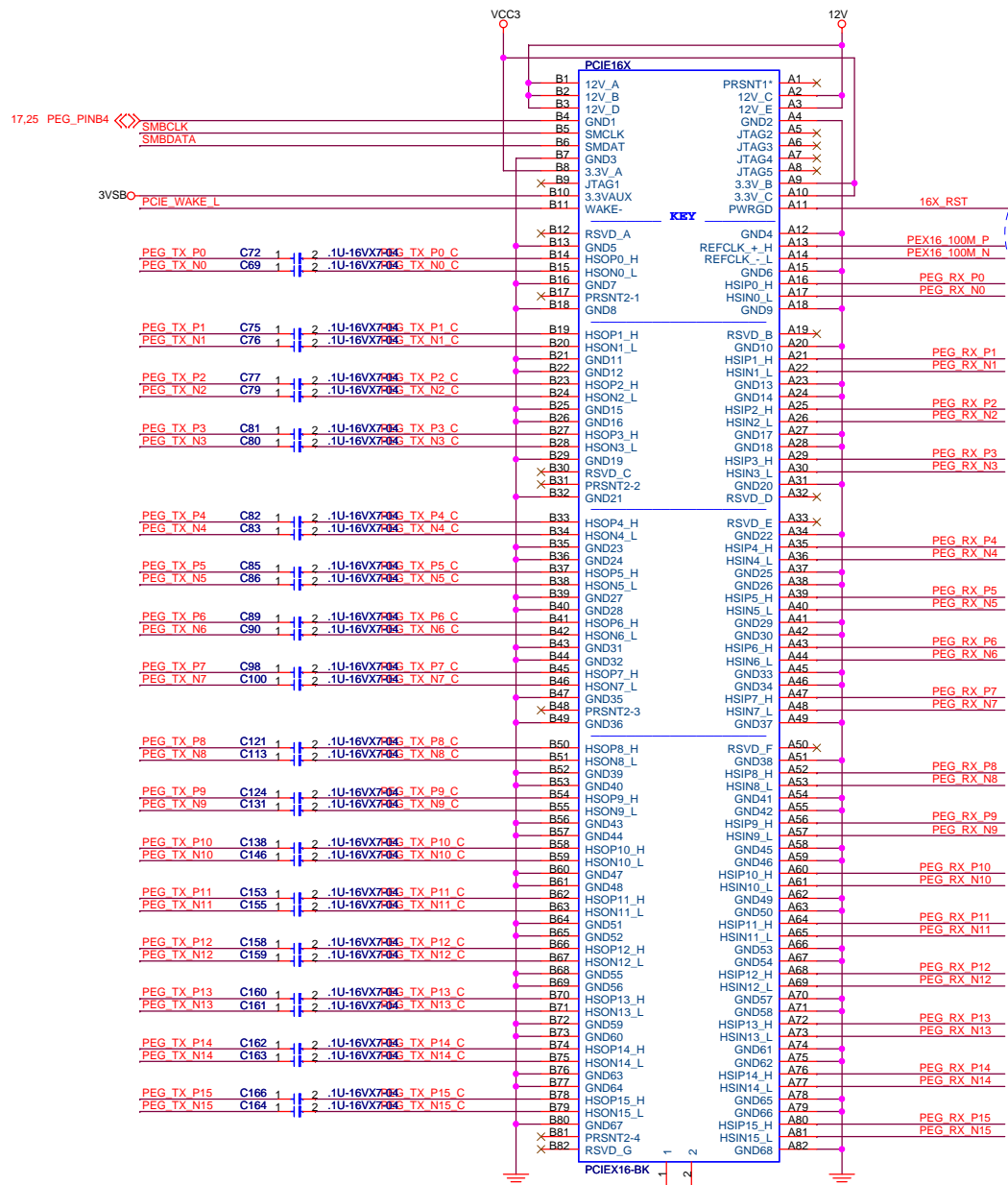
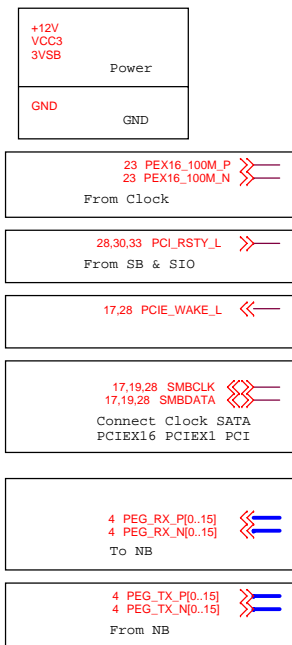
of

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6,13 M3B\_DQS7\_N  
6,13 M3B\_DQS7\_P  
6,13 M3B\_DQS6\_N  
6,13 M3B\_DQS6\_P  
6,13 M3B\_DQS5\_N  
6,13 M3B\_DQS5\_P  
6,13 M3B\_DQS4\_N  
6,13 M3B\_DQS4\_P  
6,13 M3B\_DQS3\_N  
6,13 M3B\_DQS3\_P  
6,13 M3B\_DQS2\_N  
6,13 M3B\_DQS2\_P  
6,13 M3B\_DQS1\_N  
6,13 M3B\_DQS1\_P  
6,13 M3B\_DQS0\_N  
6,13 M3B\_DQS0\_P

M3B\_DQS7\_N  
M3B\_DQS7\_P  
M3B\_DQS6\_N  
M3B\_DQS6\_P  
M3B\_DQS5\_N  
M3B\_DQS5\_P  
M3B\_DQS4\_N  
M3B\_DQS4\_P  
M3B\_DQS3\_N  
M3B\_DQS3\_P  
M3B\_DQS2\_N  
M3B\_DQS2\_P  
M3B\_DQS1\_N  
M3B\_DQS1\_P  
M3B\_DQS0\_N  
M3B\_DQS0\_P

M3B\_ODT2  
M3B\_ODT3

RSVD  
ODT1  
ODT0  
NC/PAIR IN  
NC/TEST4  
NC/TEST4

VTT\_DDR

# CHANNEL B DIMM1

13 DIMM\_CA\_VREF\_B  
13 DIMM\_DQ\_VREF\_B  
11,12,13,19,27,41 SCLK  
11,12,13,19,27,41 SDATA

DIMM CA VREF B  
DIMM DQ VREF B  
SCLK  
SDATA

6,13 M3B\_D[63.0]

6,13 M3B\_DM[7.0]

M3B\_DM0  
M3B\_DM1  
M3B\_DM2  
M3B\_DM3  
M3B\_DM4  
M3B\_DM5  
M3B\_DM6  
M3B\_DM7  
M3B\_DM8

M3B\_D0  
M3B\_D1  
M3B\_D2  
M3B\_D3  
M3B\_D4  
M3B\_D5  
M3B\_D6  
M3B\_D7  
M3B\_D8  
M3B\_D9  
M3B\_D10  
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M3B\_D62  
M3B\_D63

DIMM8

DDR3-240P-GR

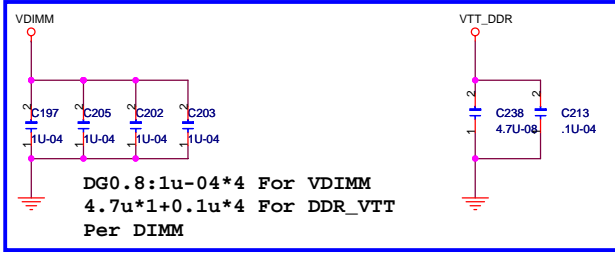
M3B\_WEB  
M3B\_RASB  
M3B\_CASB  
6,13  
6,13

DDR3\_DRAMRST\_L 5,11,12,13

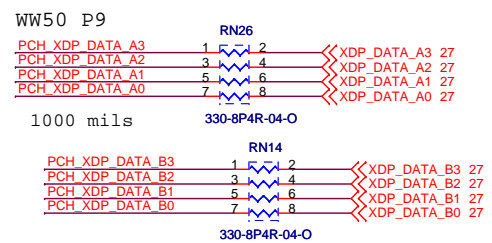
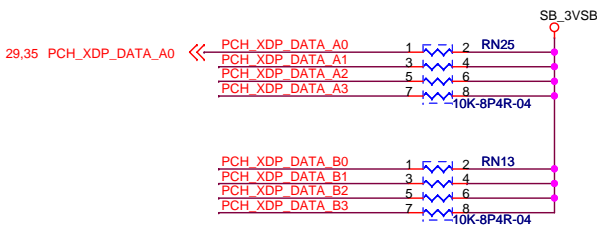
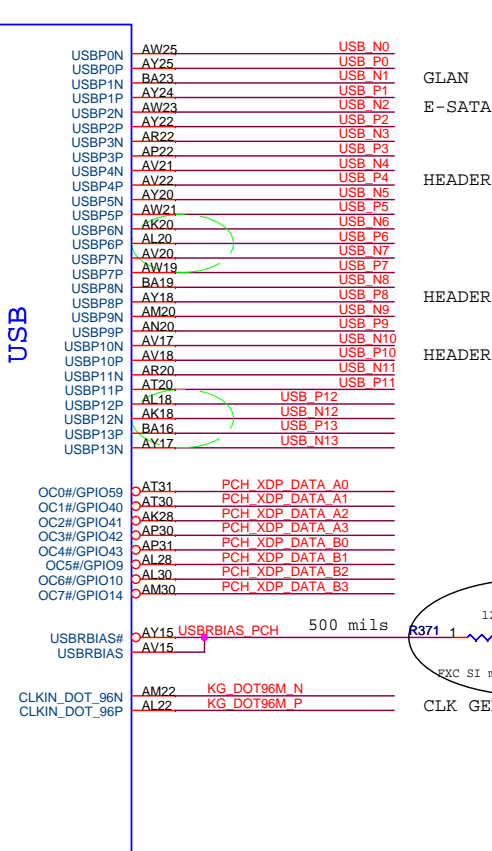
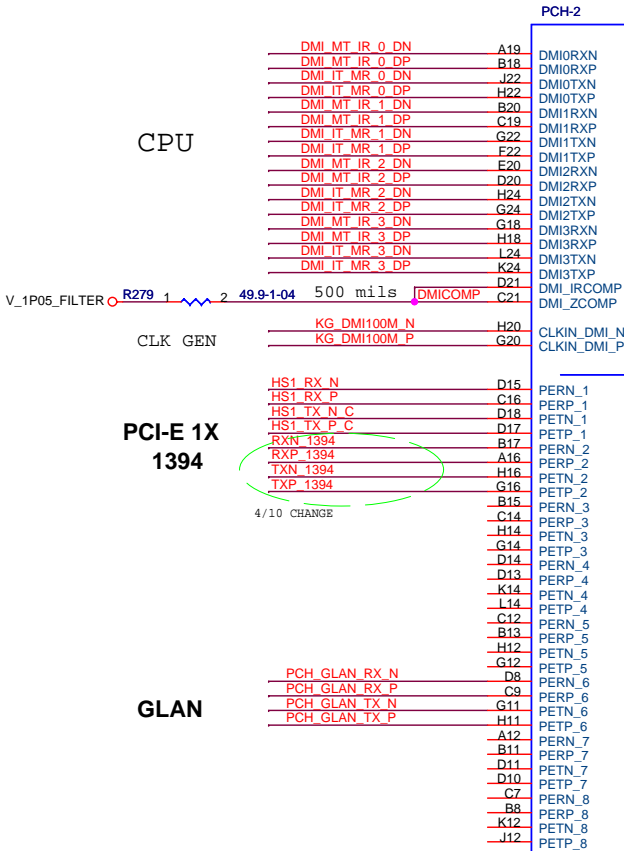
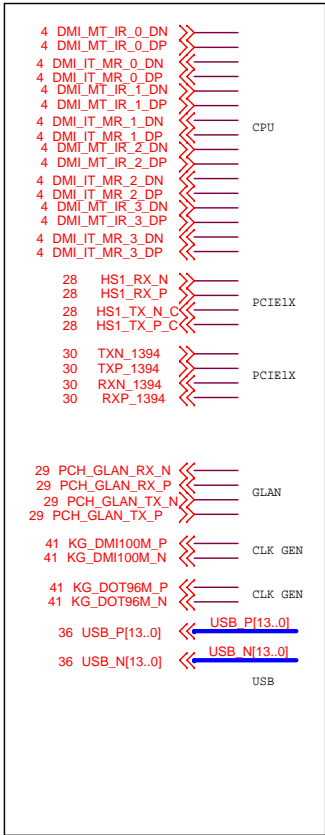
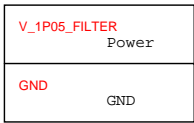
M3B\_CK2\_P 6  
M3B\_CK2\_N 6  
M3B\_CK3\_P 6  
M3B\_CK3\_N 6

6,13 M3B\_MA[15.0]

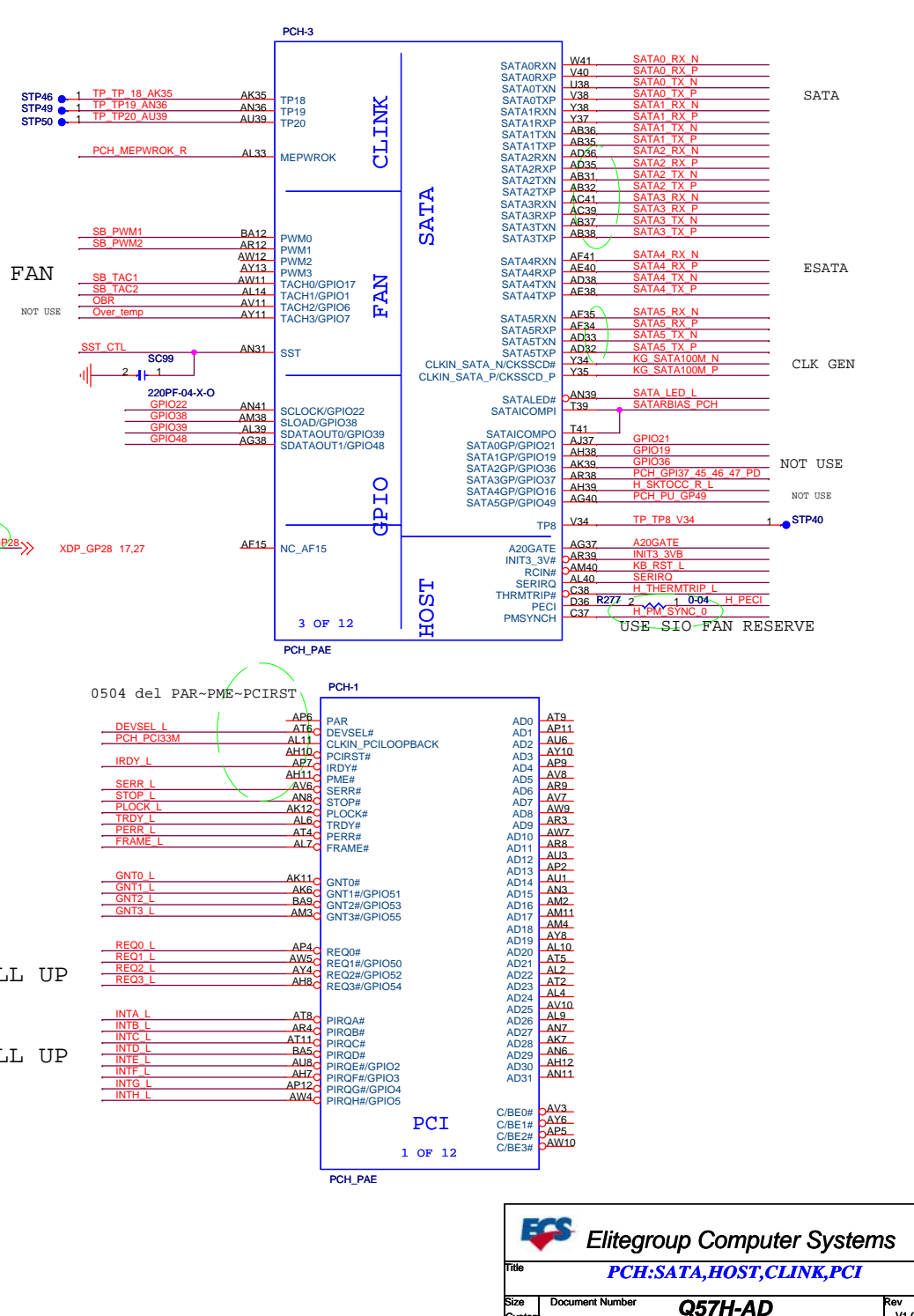
6,13 M3B\_ODT[3.0]  
6,13 M3B\_CSB[3.0]  
6,13 M3B\_CKE[3.0]  
6,13 M3B\_BS[2.0]



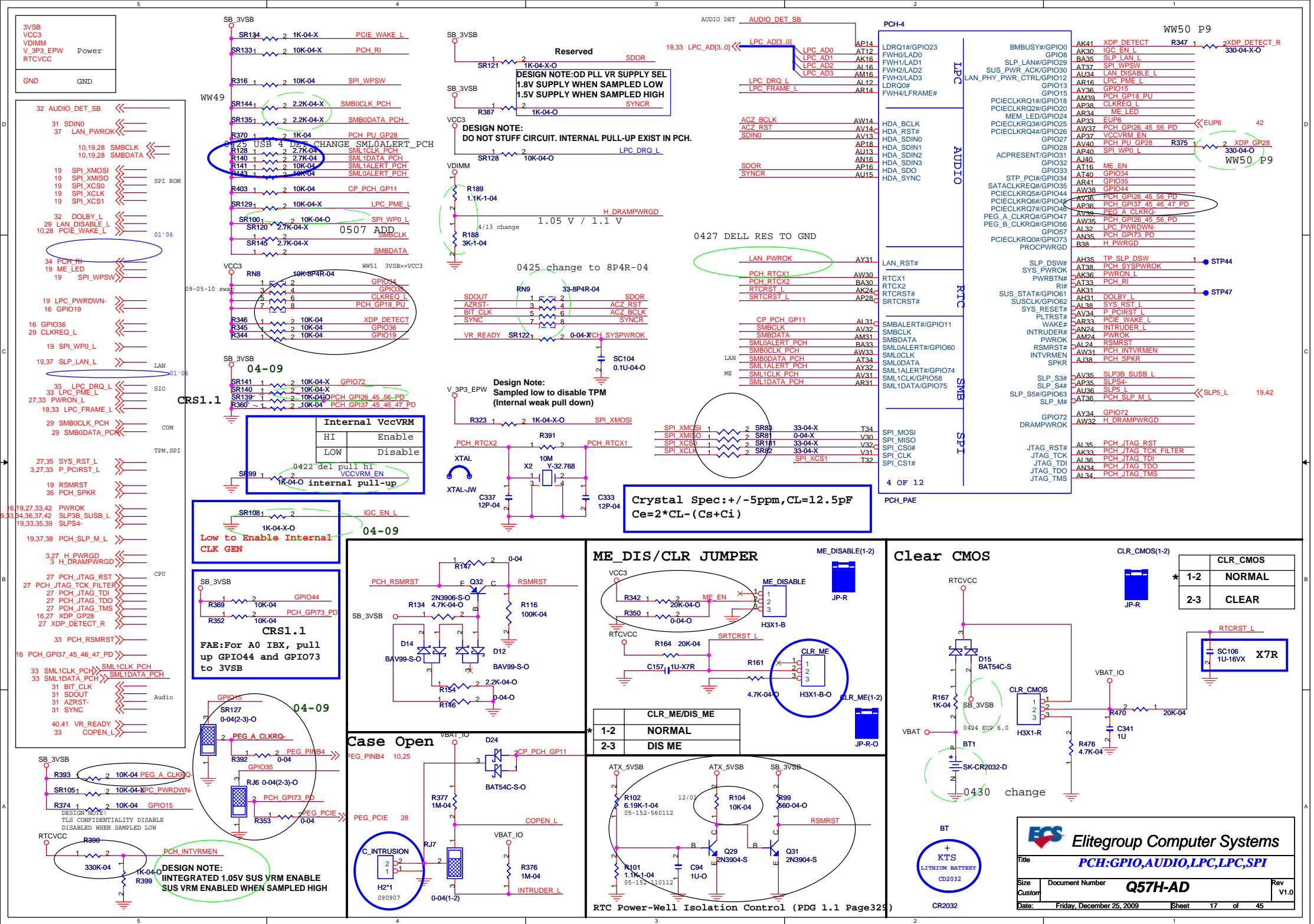
DDR_VTT VDIMM DIMM_VDDSPD	Power
GND	GND







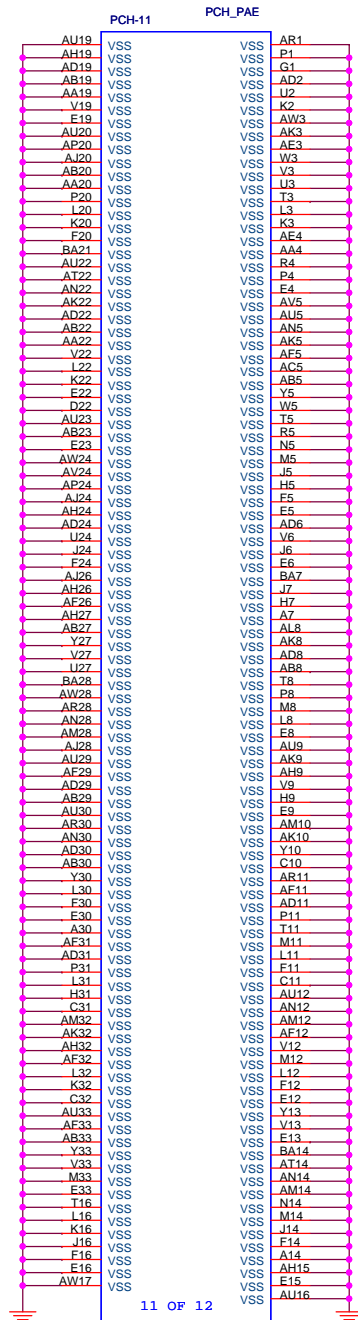




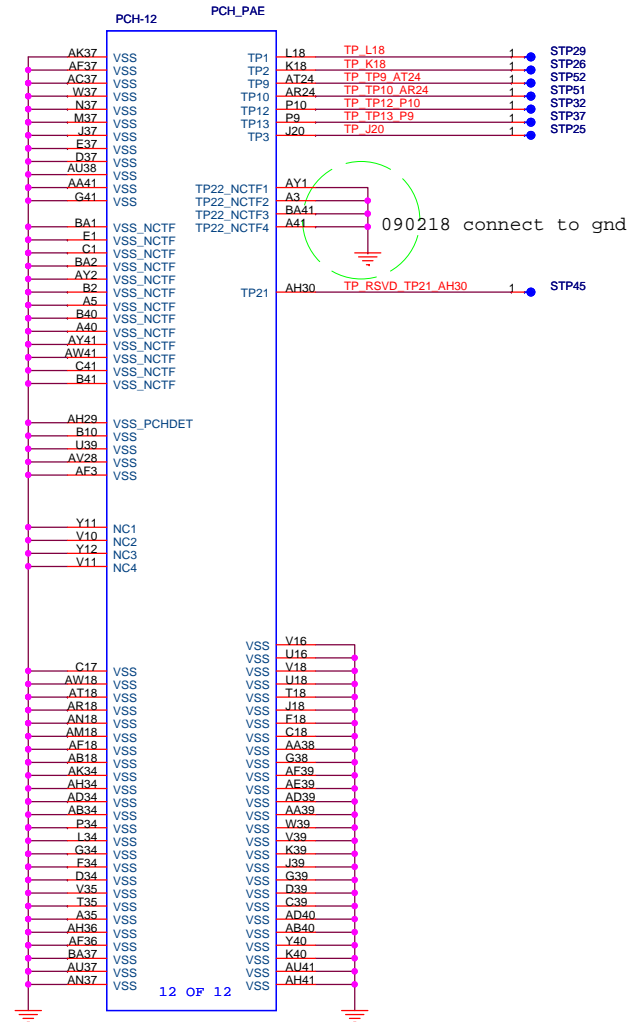


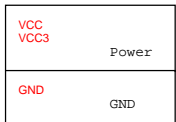






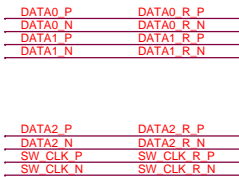
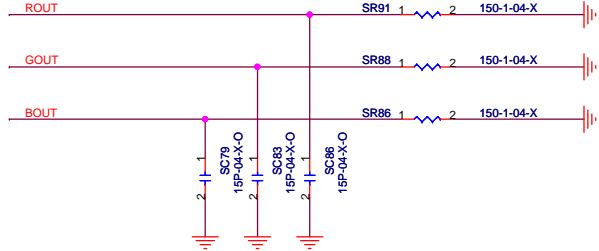
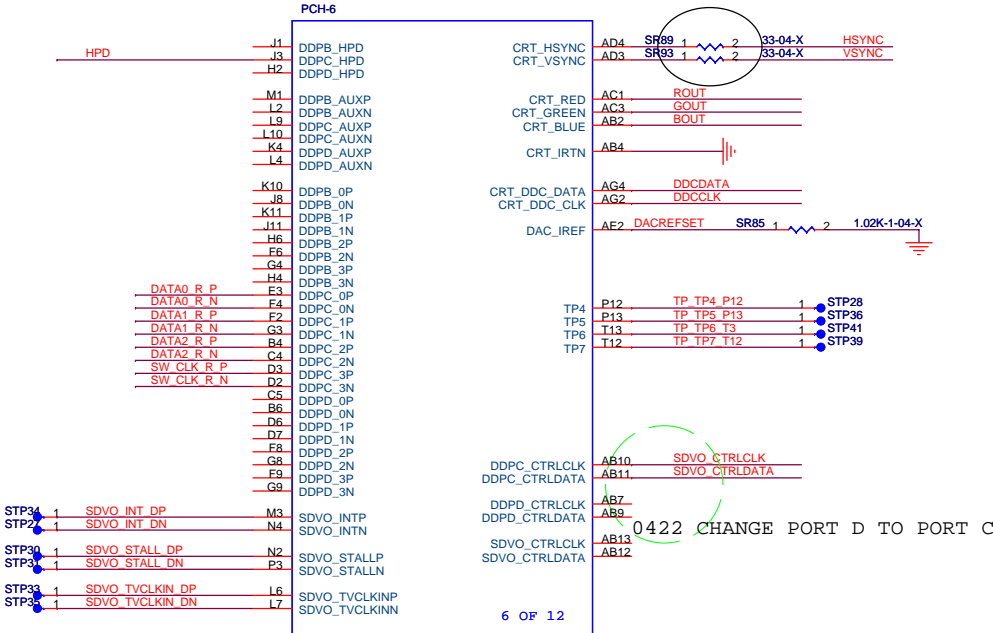
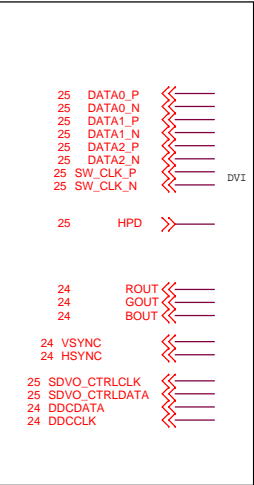
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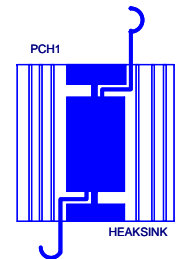
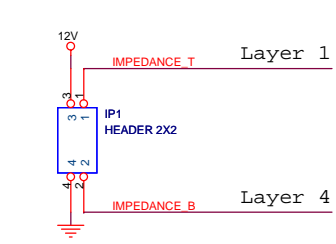
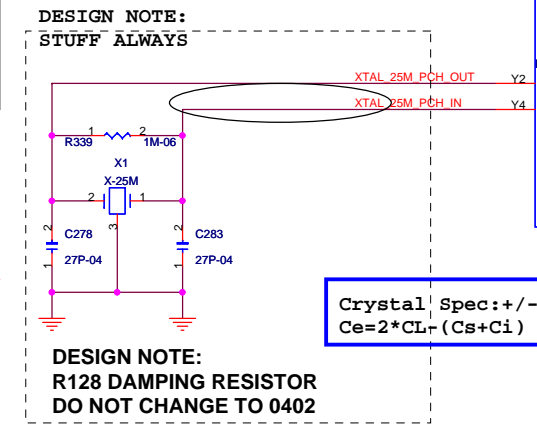
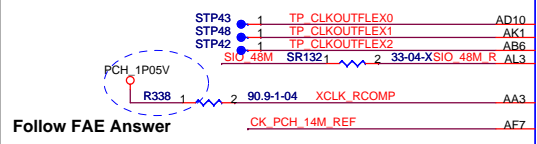
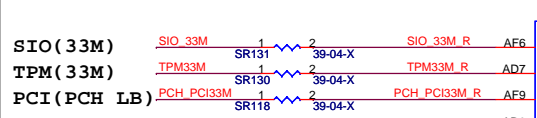
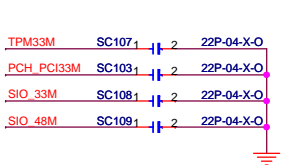
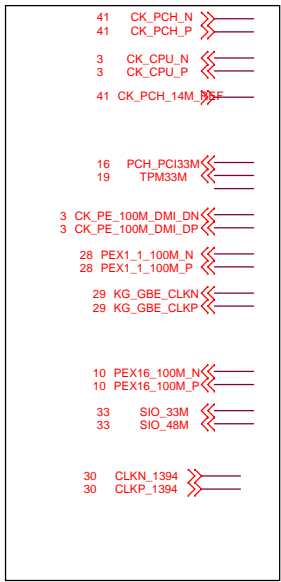
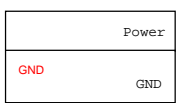




(WW07 DVI-I ONLY PORT B)

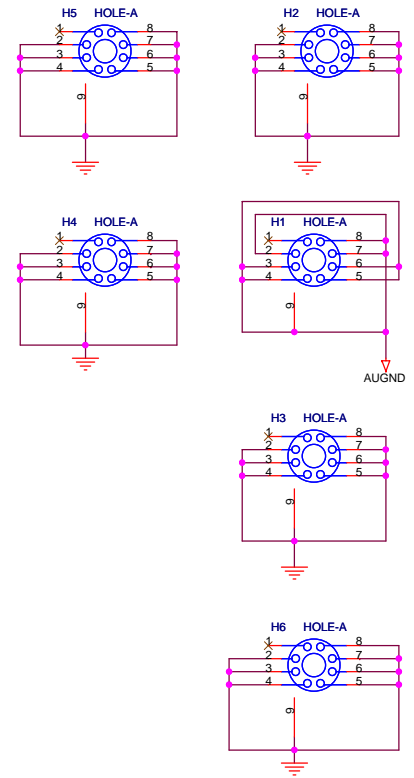
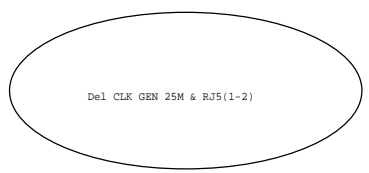
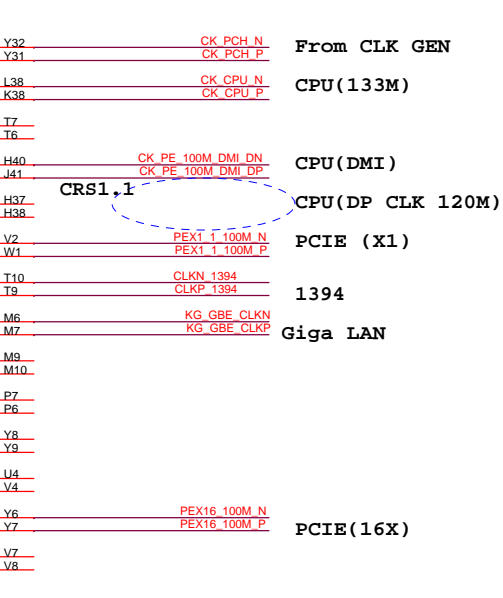
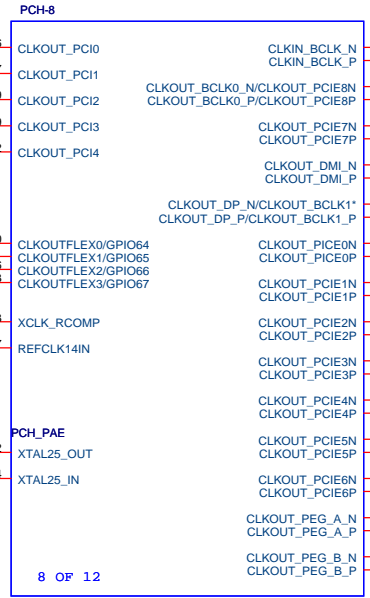
Port B:Capable of SDVO/HDMI/DVI/DP  
Port C:Capable of HDMI/DVI/DP  
Port D:Capable of HDMI/DVI/DP





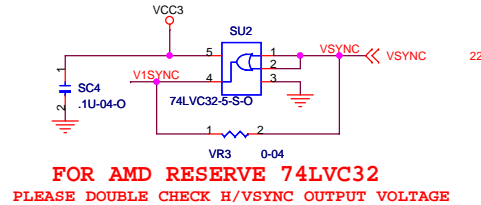
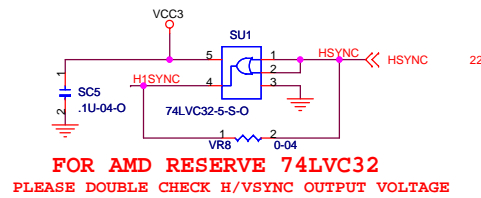
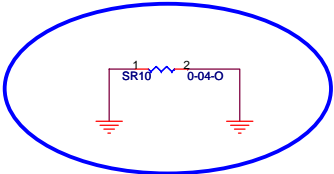
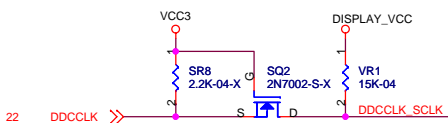
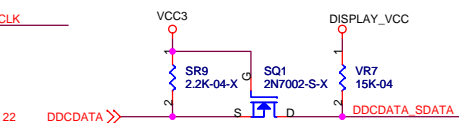
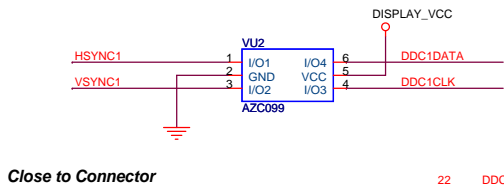
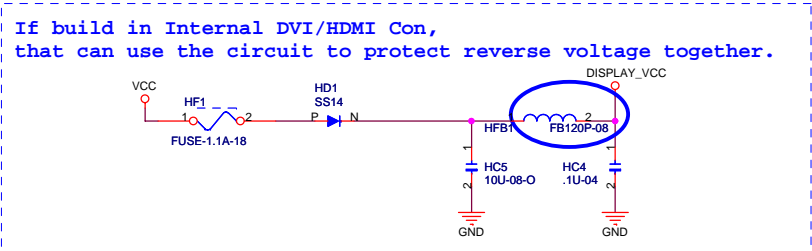
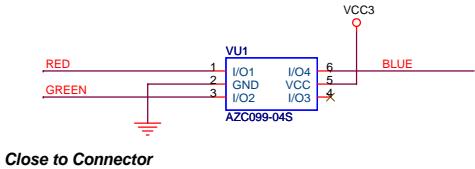
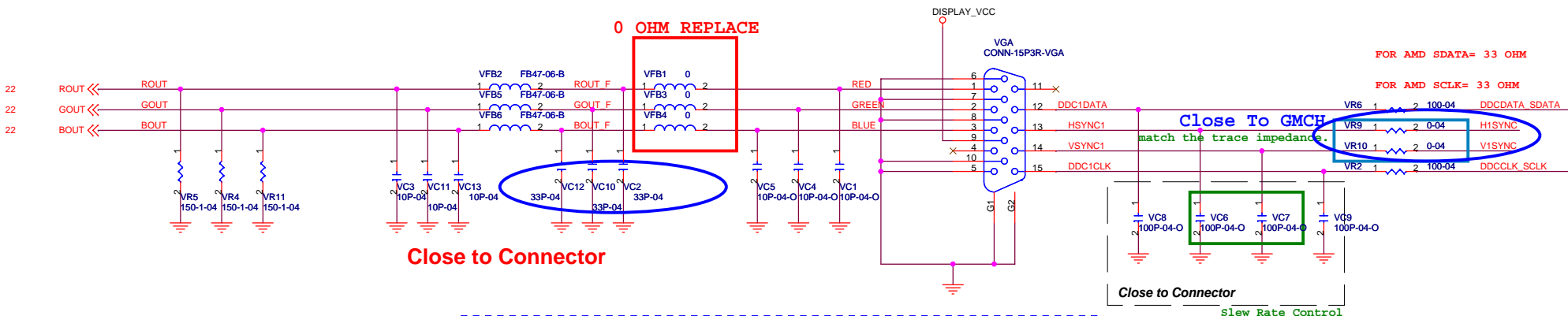
Main Part:20-120-014500

1080 : trace width 4 mil 50 ohm  
Trace Length 3150 mils  
Spacing: 1.clearance to itself 50/4/50(S:W:S)  
2.clearance to other signal 3W

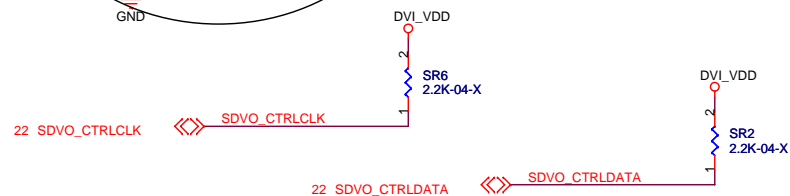




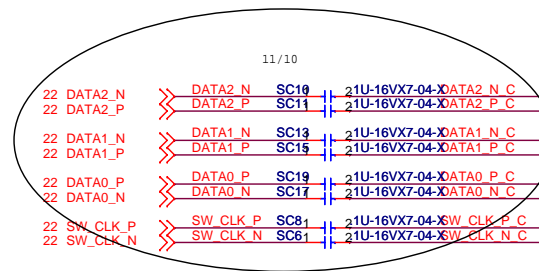
VGA Connector



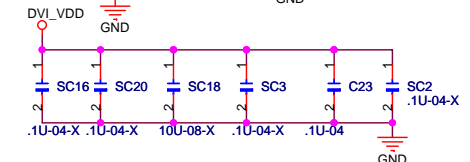
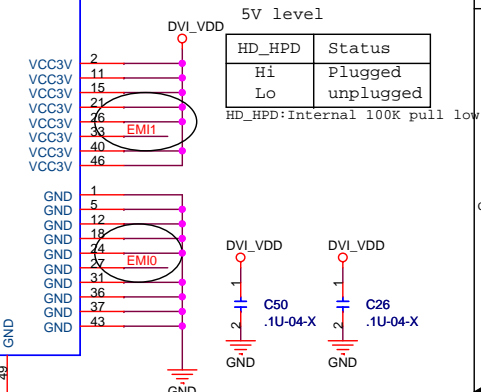
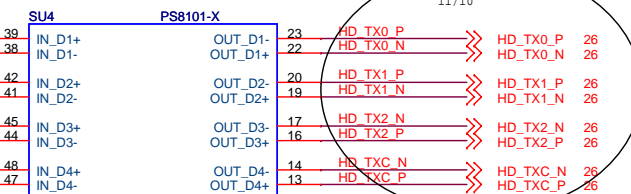
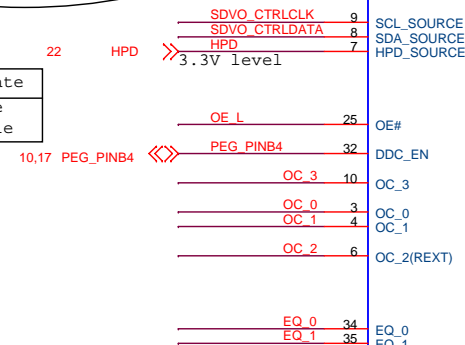




	PS8101	PI3VDP411LST2DES
EQ_0	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
EQ_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_0	4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_2	499 1% OHM PULL DOWN	RESERVE 4.7K PULL DOWN
OC_3	NC	RESERVE 4.7K PULL DOWN
PEG_PINB4	RESERVE 4.7K PULL UP	NC
HR20	NC	20K-04



DDC_EN	Passgate
3.3V	Enable
0	Disable



FOR PS8101

	OC_0	OC_1	Equalization(dB)
*	0	0	8
	0	1	4
	1	0	12
	1	1	0

FOR PI3VDP411LSTZDES

	OC_3	OC_2	OC_1	OC_0	Vswing(mV)	Pre/De-emphasis
*	0	0	0	0	500	0
	0	0	0	1	600	0
	0	0	1	0	750	0
	.	.	.	.		

	EQ_0	EQ_1	Equalization(dB)
*	0	0	3
	0	1	7.2
	1	0	10
	1	1	20



Title	<b><i>HDMI Interface (Switch, Level shifter)</i></b>
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5 4 3 2 1

D

D

C

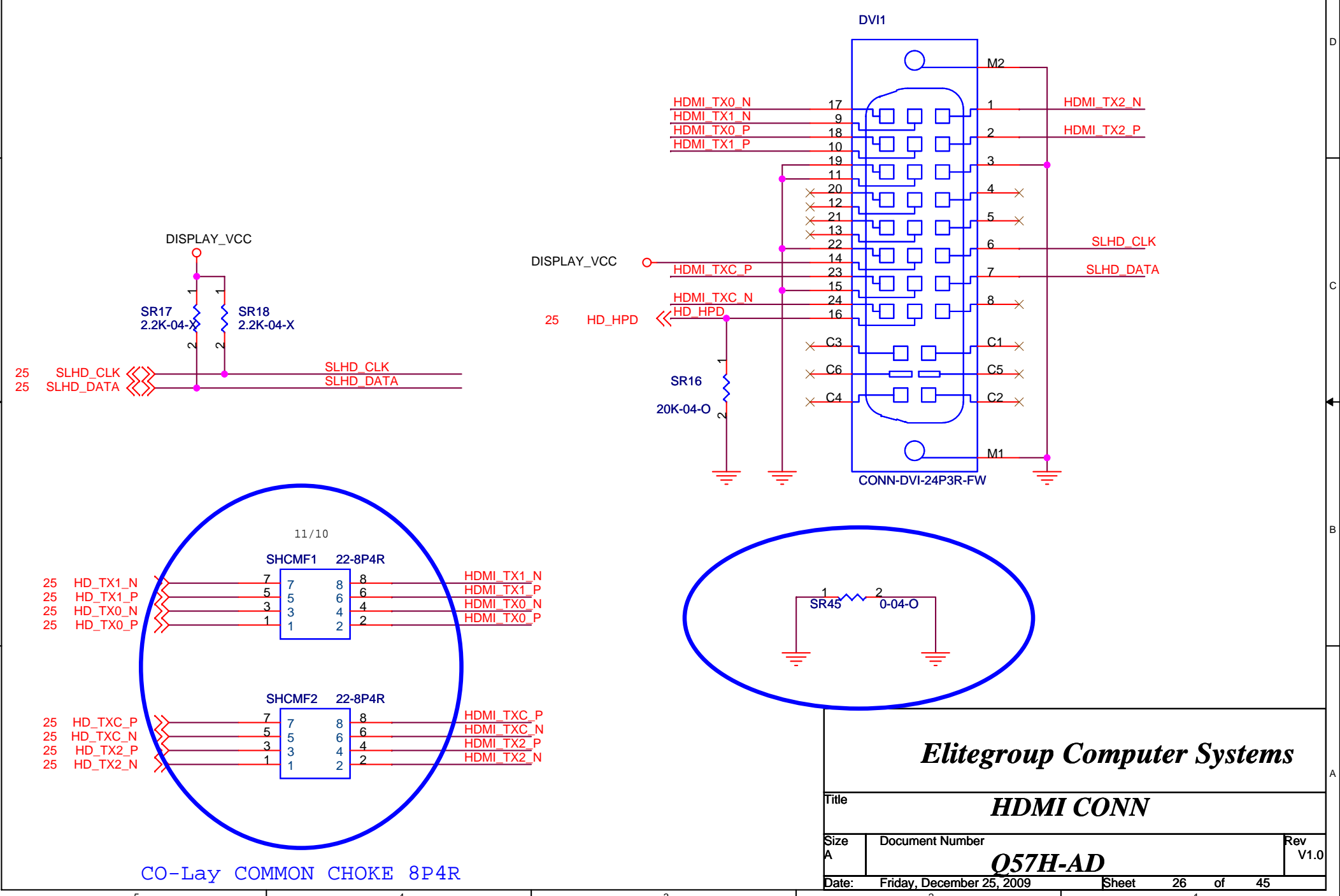
C

B

B

A

A

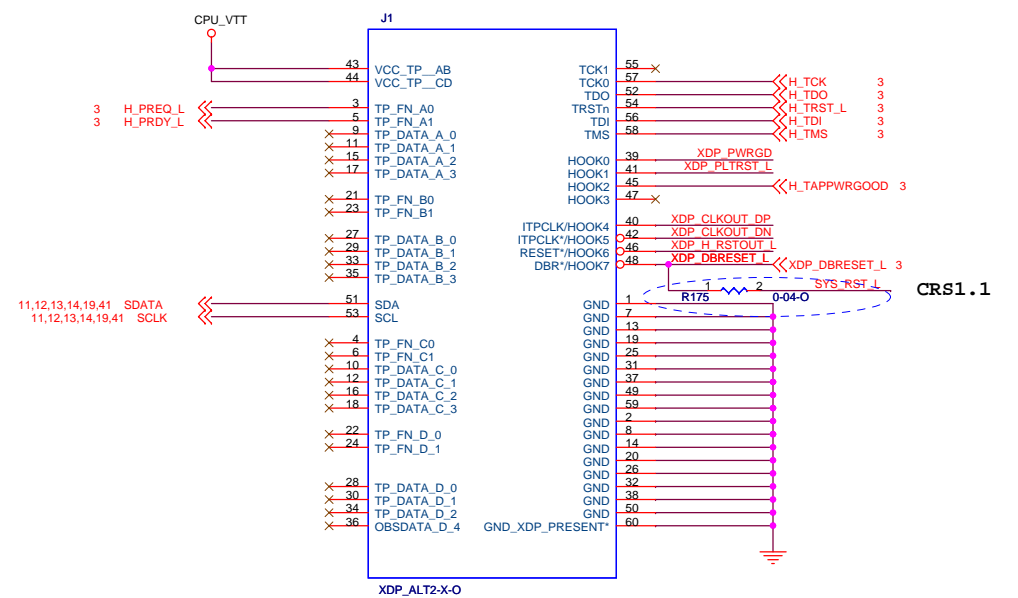
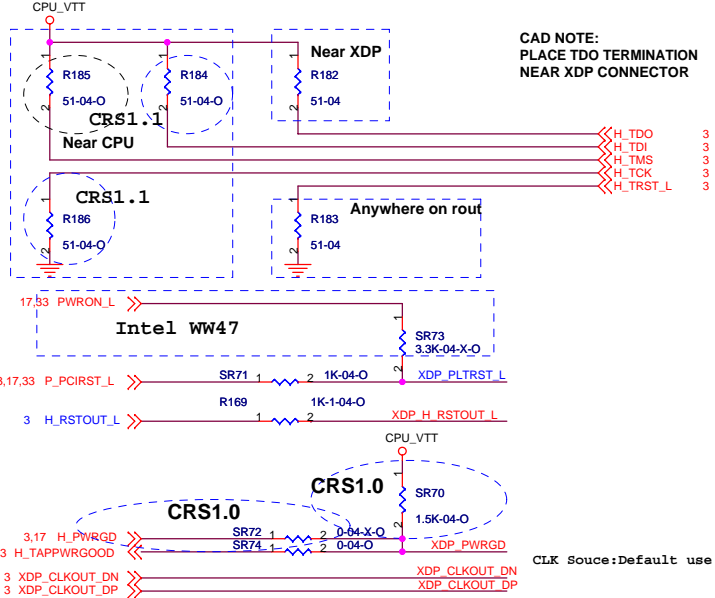


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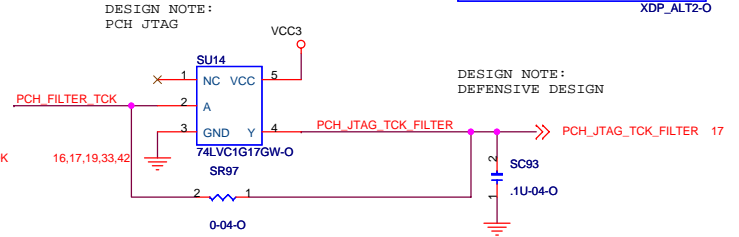
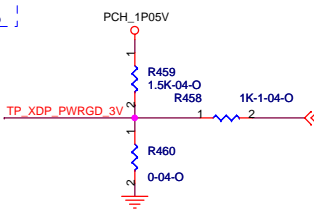
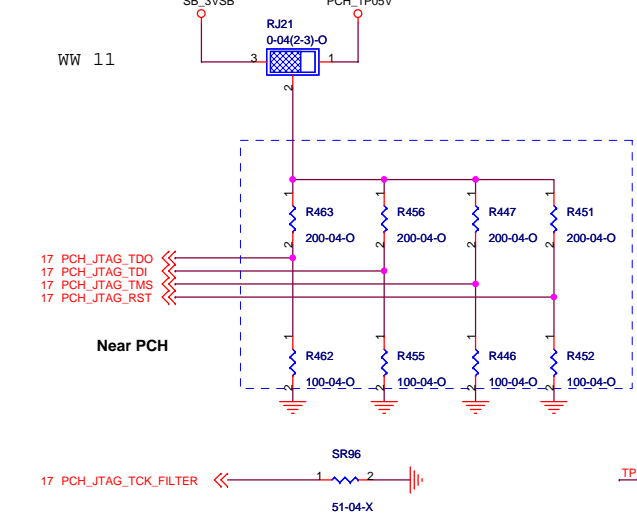
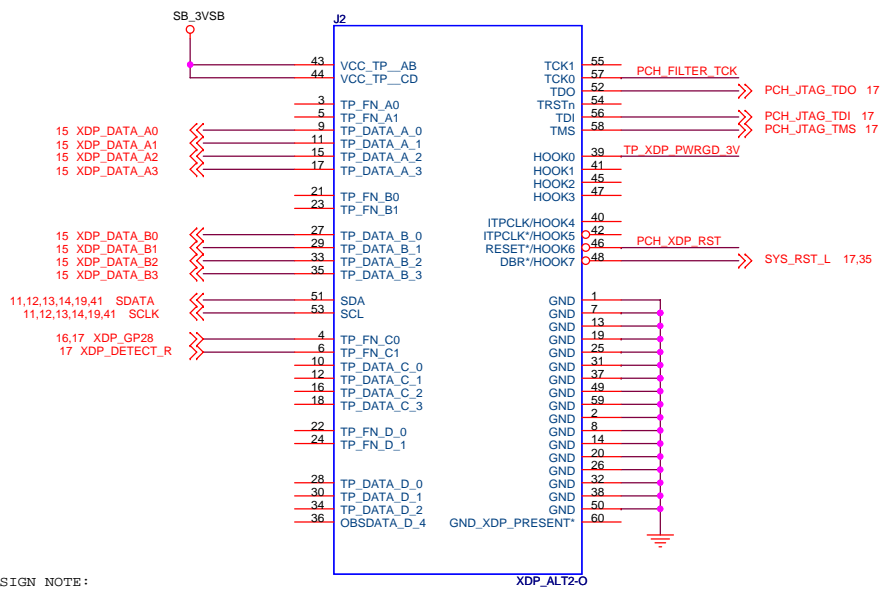
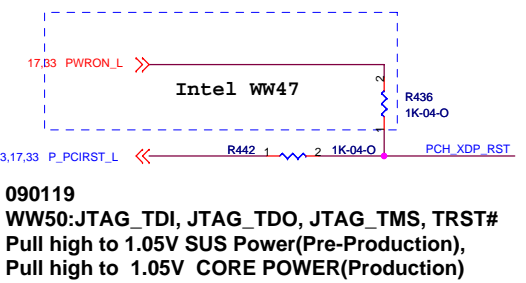
Title **HDMI CONN**

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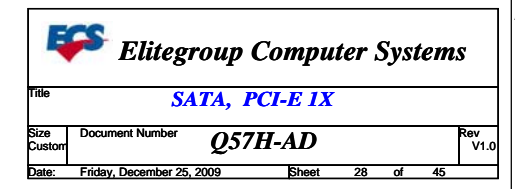
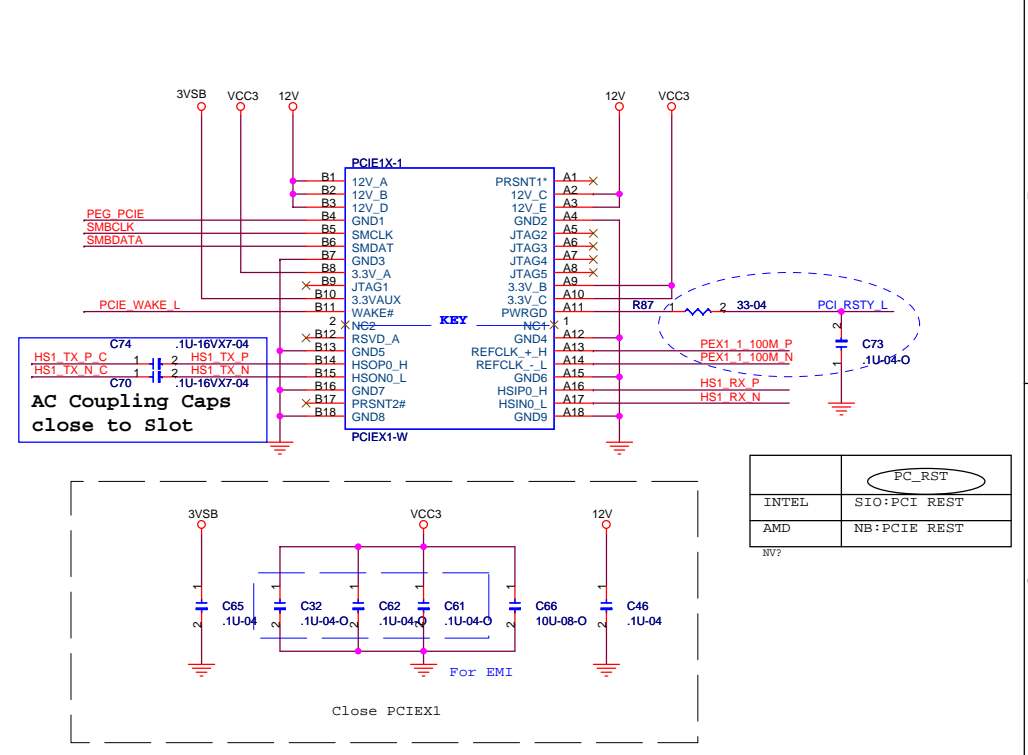
DESIGN NOTE:  
DEFAULT EMPTY SITE ON PAGE 94: XDP\_PWRGD RES (R108PR) TO VTT\_OUT\_RIGHT  
DEFAULT EMPTY SITE ON PAGE 123: XDP\_PWRGD RES (R3S3EV) TO V\_FSB\_VTT  
DEFAULT STUFF SITE: (R662EV) TO TP\_XDP\_PWRGD

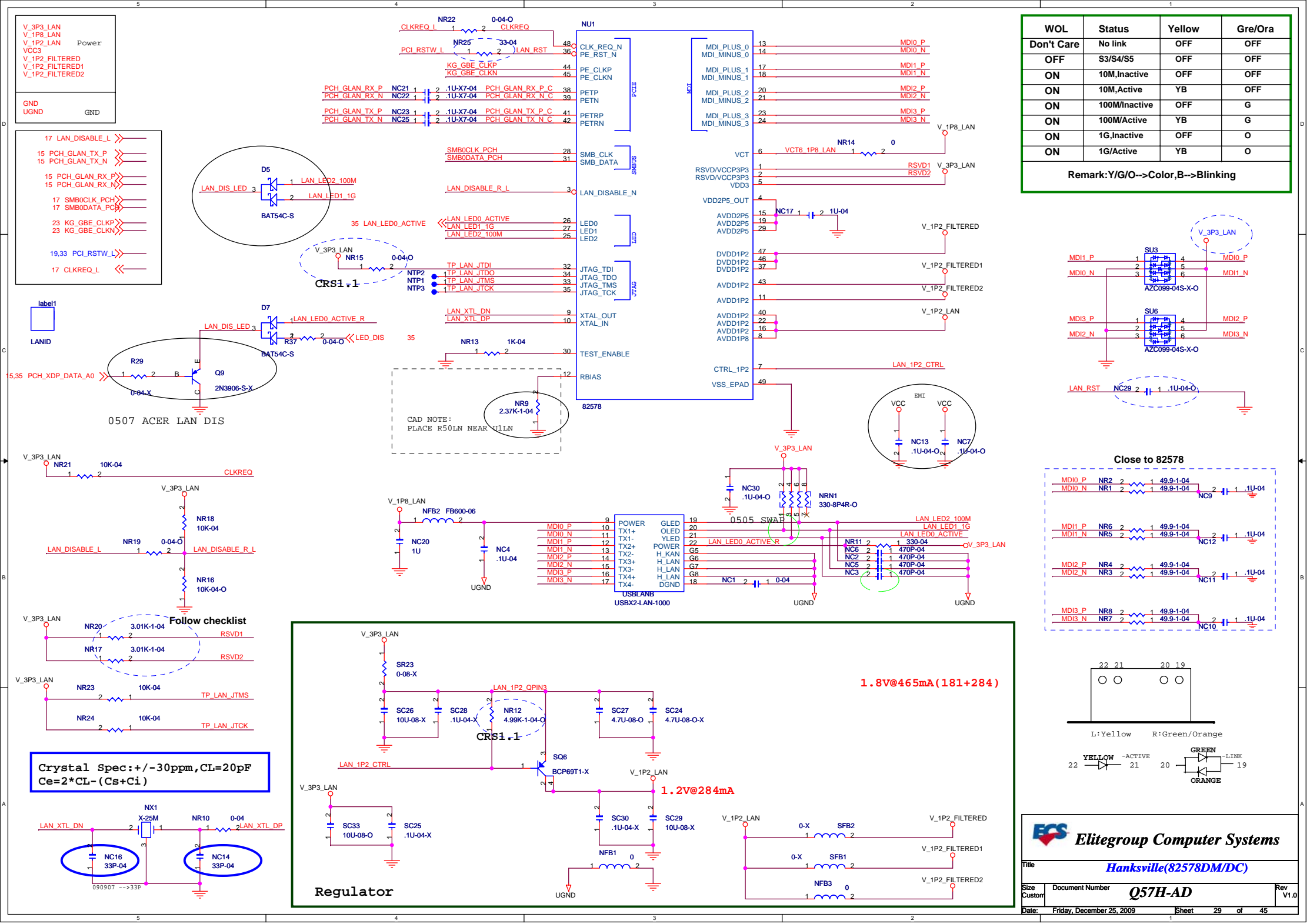


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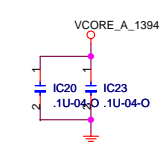
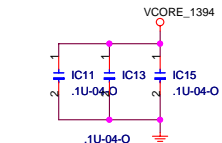
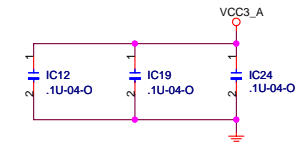
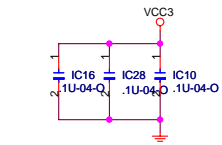
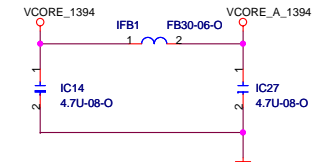
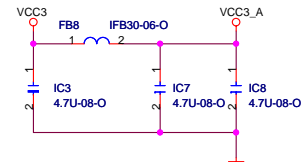
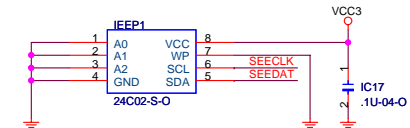
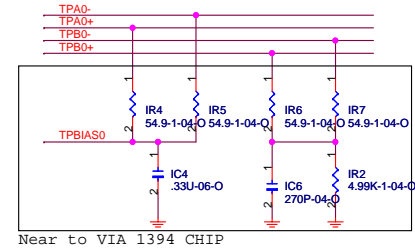
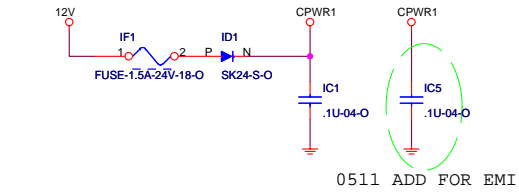
**Primary&PCH XDP**

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		<b>Q57H-AD</b>		V1.0
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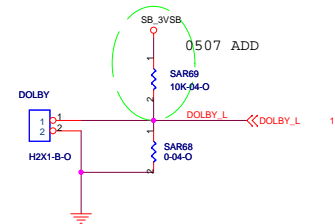
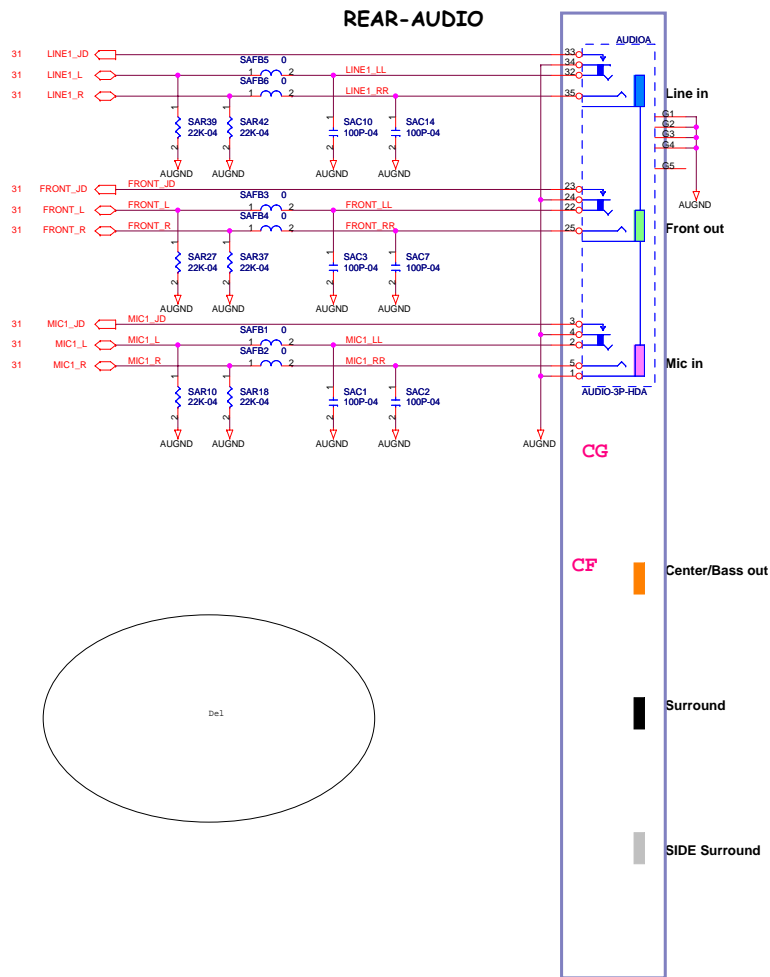




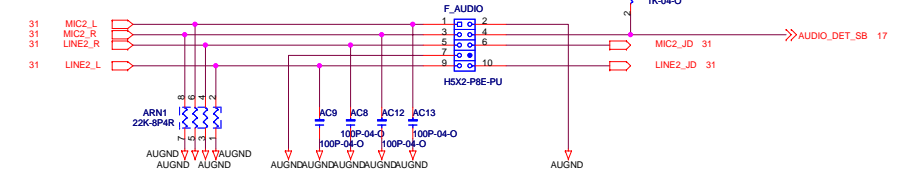
shadow EEPROM	ON	OFF
R215	V	X



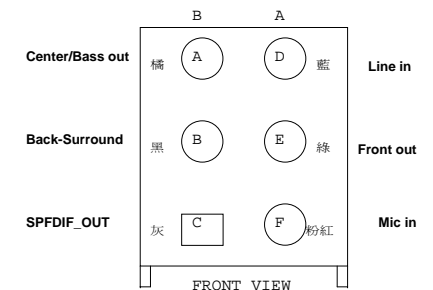
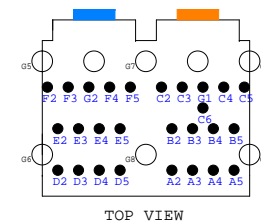
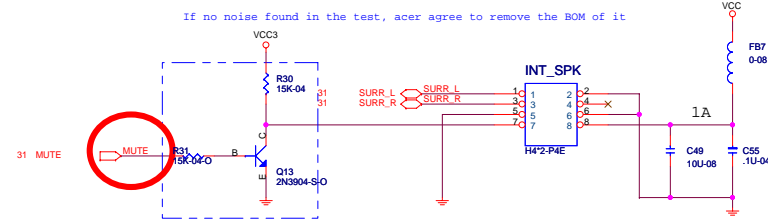
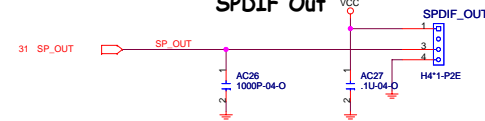




### FRONT-AUDIO

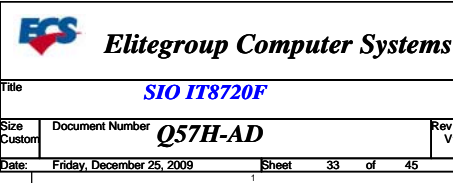


### SPDIF Out

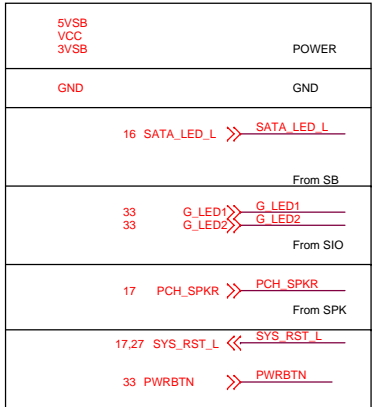


GPI: cable detection	
LOW	Plug cable
HIGH	No plug cable





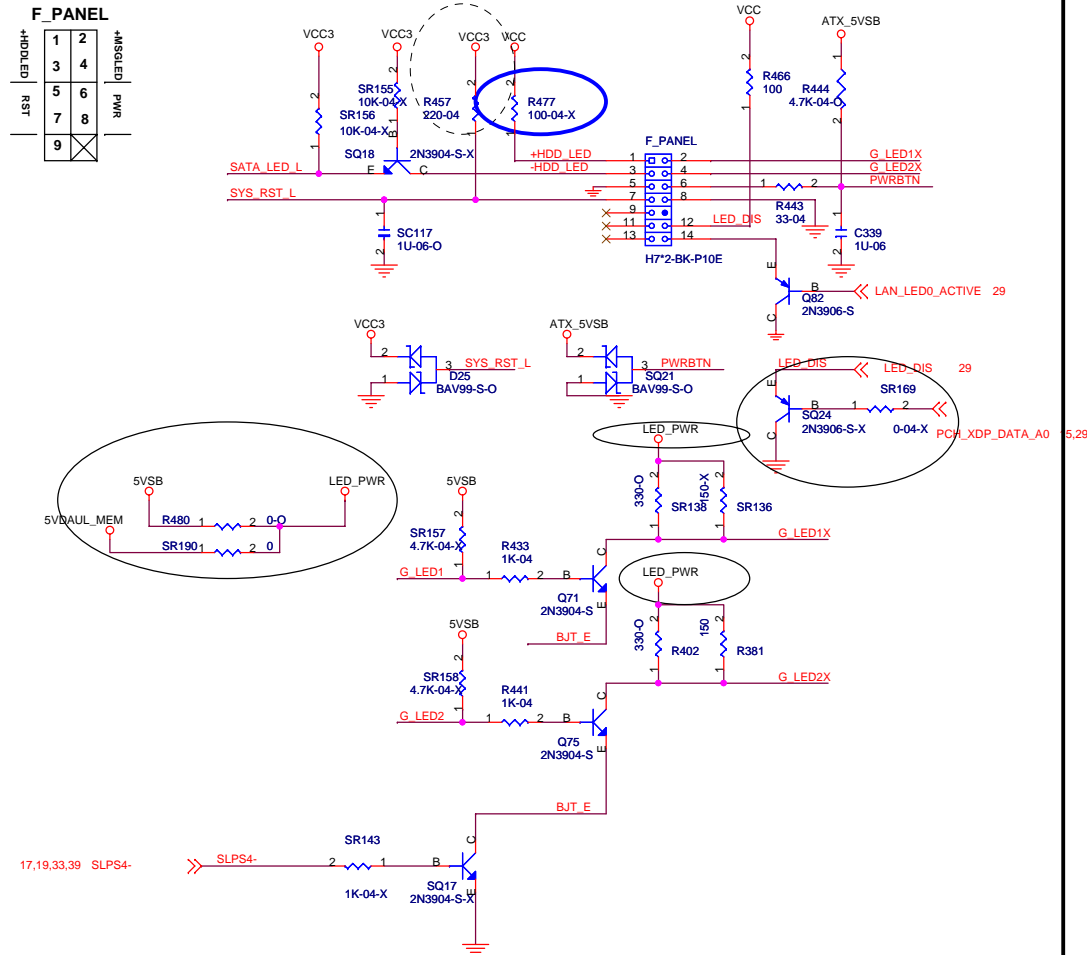




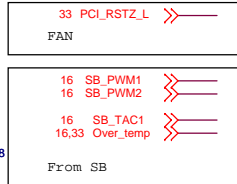
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
Status	G	GB	YB	OFF	OFF
Remark	B:Blinking				

090119  
WW51 SYS\_RST\_L should  
pull high to VCC3 not 3VSB and 220 ohm

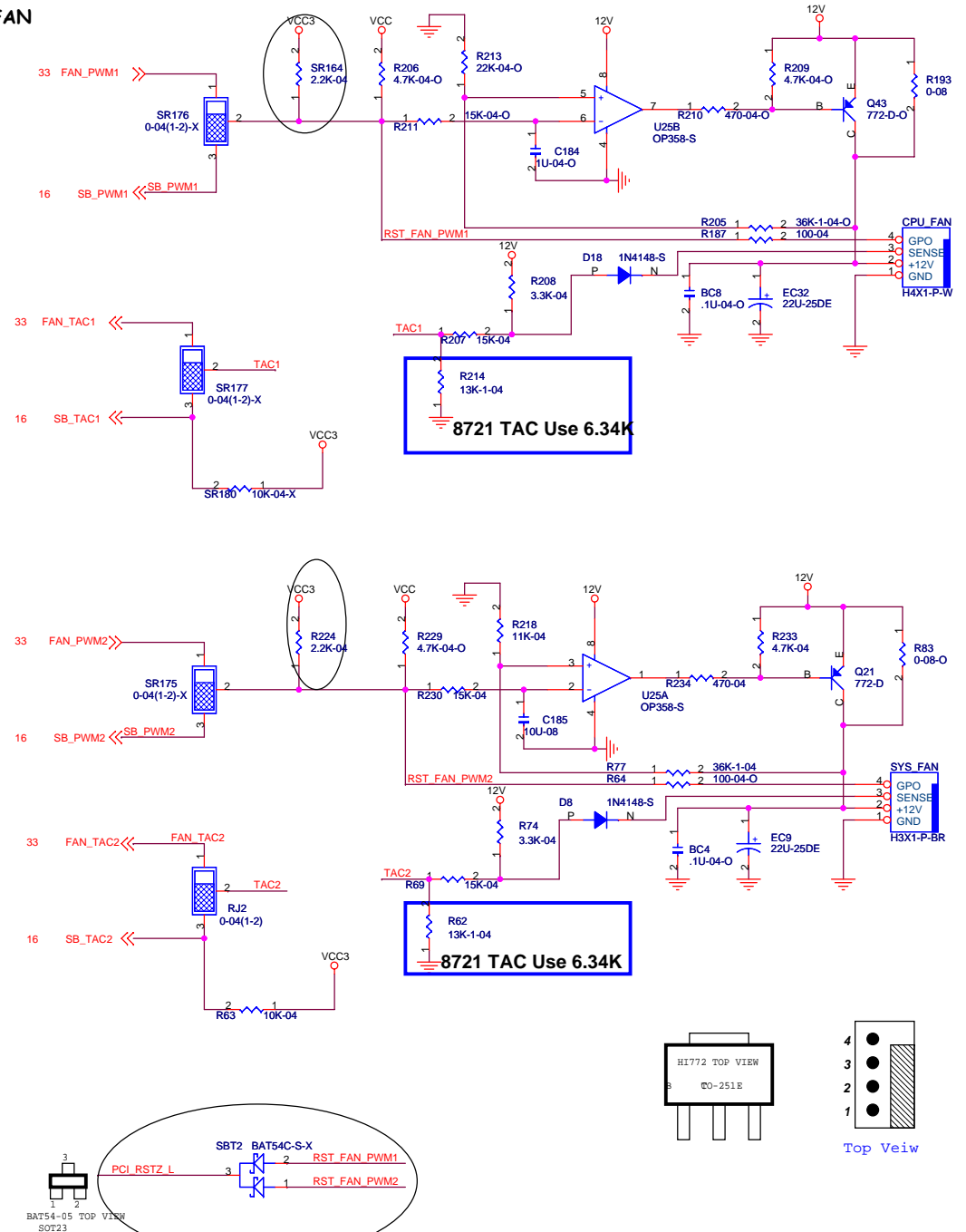
F_PANEL		
+HDDLED	1	2
	3	4
	5	6
	7	8
	9	X
		PWR

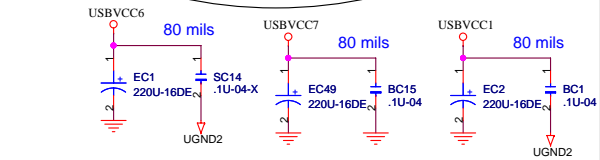
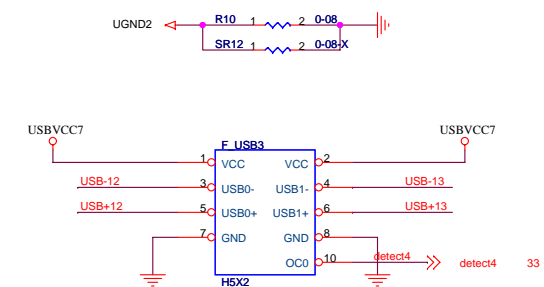
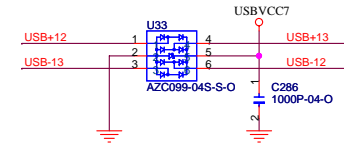
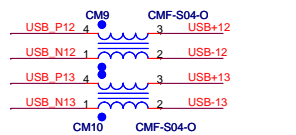
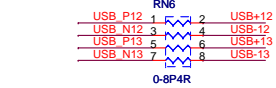


## PANEL

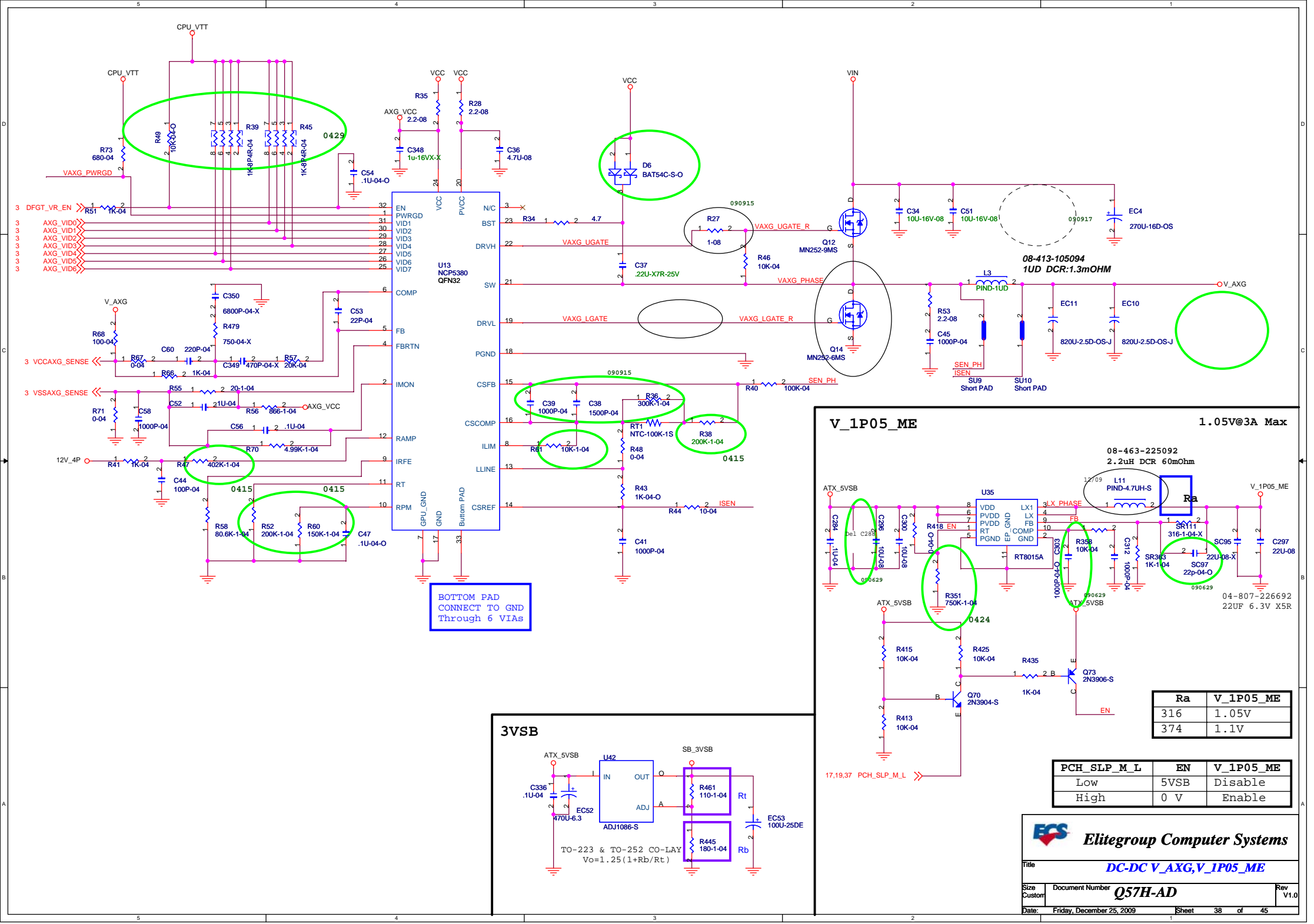


## FAN











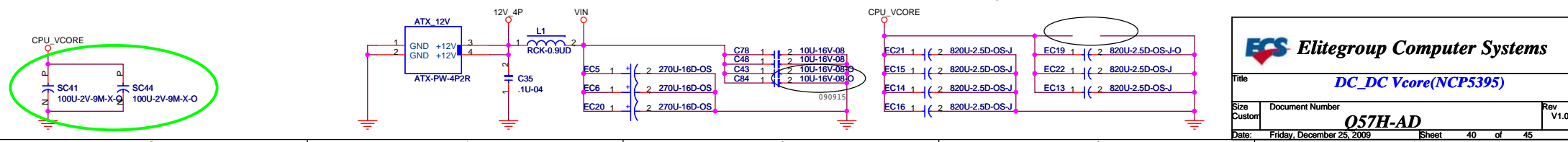
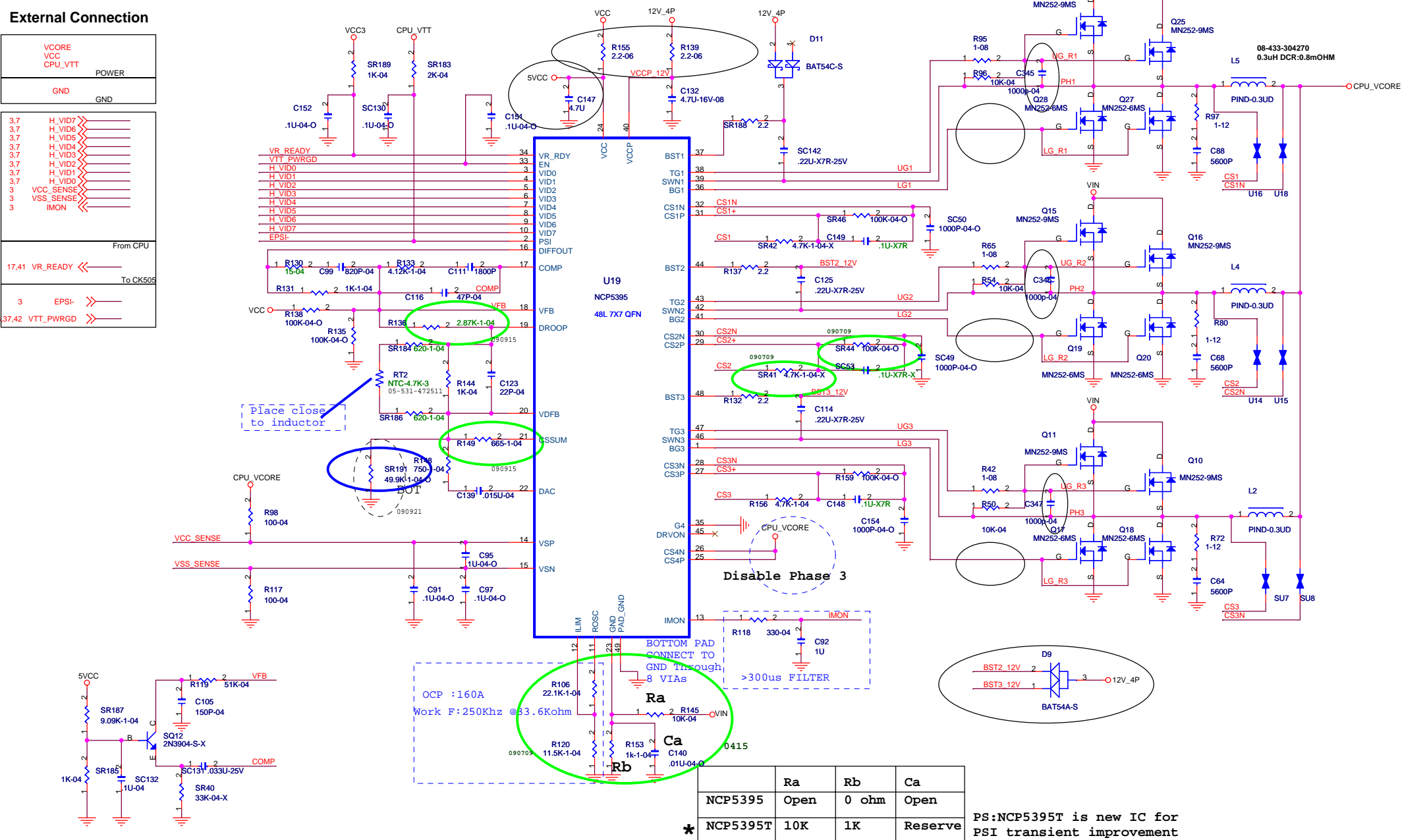


## External Connection

VCCORE VCC CPU_VTT	POWER
GND	GND

3,7	H_VID7
3,7	H_VID6
3,7	H_VID5
3,7	H_VID4
3,7	H_VID3
3,7	H_VID2
3,7	H_VID1
3,7	H_VID0
3	VCC_SENSE
3	VSS_SENSE
3	IMON

From CPU	
17,41	VR_READY <<—
To CK505	
3	EPSI- >>—
3,37,42	VTT_PWRGD >>—

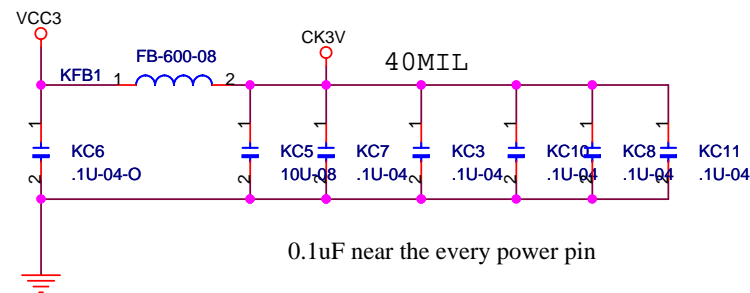
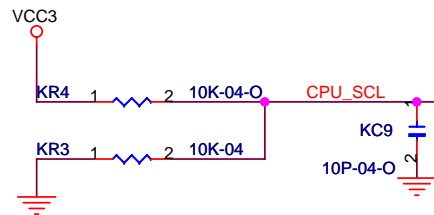
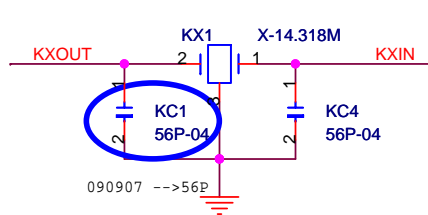
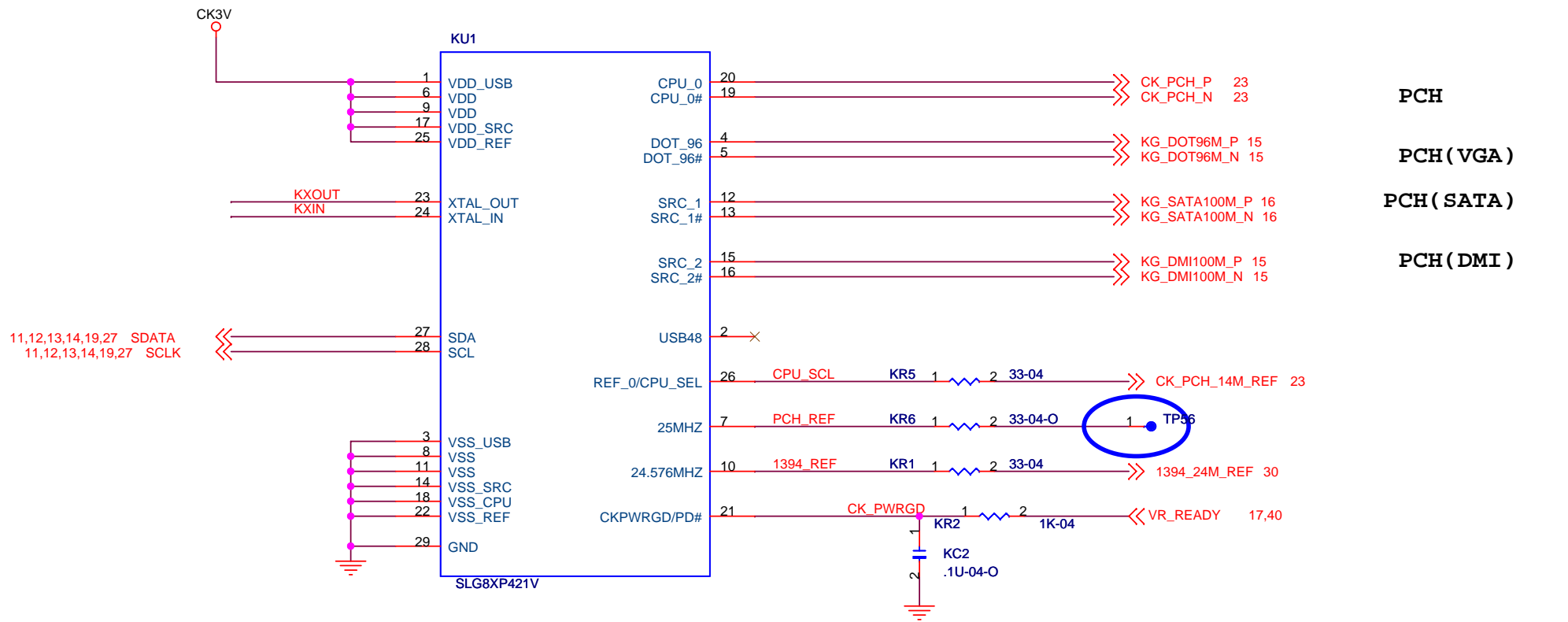


**Elitegroup Computer Systems**


DC\_DC Vcore(NCP5395)

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PIN 26	CPU_0
0 (default)	133MHz
1 (0.7-1.5V)	100MHz

**Elitegroup Computer Systems**

Title**SLG8XP421V**

SizeCustom

Document Number**Q57H-AD**

RevV1.0

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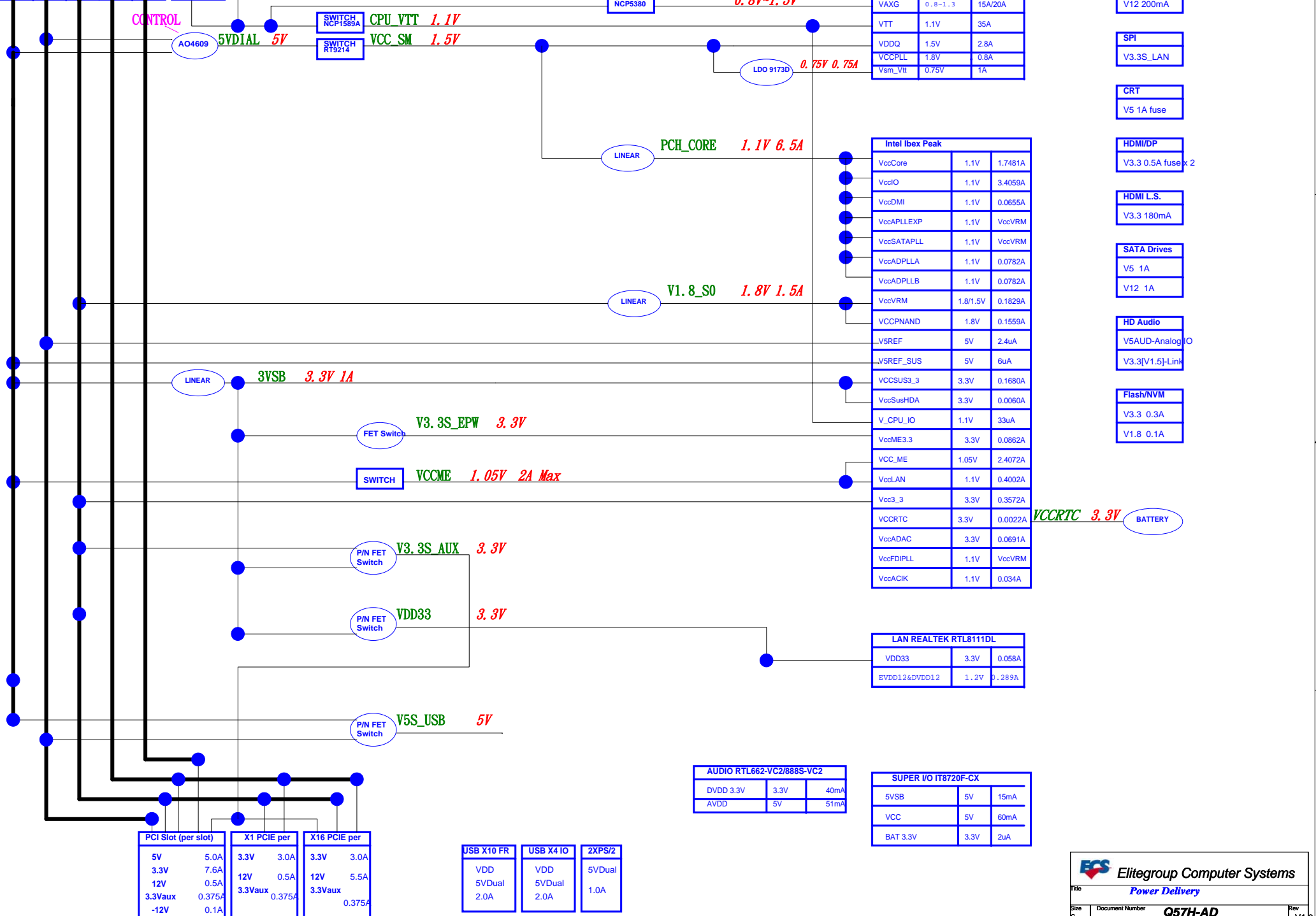
放電用的Pull Down 電阻;  
可選擇性放置,  
目的為解決漏電問題.

EUP 2009-06-22

PWROK low to VCC falling  
IBEX PEAK 40ns requirement

ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

ATX4P1
12V +/-5%



Intel Havendale/Lynnfield CPU		
VCCP	V1D 0.65~1.4	120A
VAXG	V1D 0.8~1.3	15A/20A
VTT	1.1V	35A
VDDQ	1.5V	2.8A
VCCPLL	1.8V	0.8A
Vsm_Vtt	0.75V	1A

Intel i7x Peak		
VccCore	1.1V	1.7481A
VccIO	1.1V	3.4059A
VccDMI	1.1V	0.0655A
VccAPLLEXP	1.1V	VccVRM
VccSATAPLL	1.1V	VccVRM
VccADPLLA	1.1V	0.0782A
VccADPLLB	1.1V	0.0782A
VccVRM	1.8/1.5V	0.1829A
VCCPNAND	1.8V	0.1559A
V5REF	5V	2.4uA
V5REF_SUS	5V	6uA
VCCSUS3_3	3.3V	0.1680A
VccSusHDA	3.3V	0.0060A
V_CPU_IO	1.1V	33uA
VccME3.3	3.3V	0.0862A
VCC_ME	1.05V	2.4072A
VccLAN	1.1V	0.4002A
Vcc3_3	3.3V	0.3572A
VCCRTC	3.3V	0.0022A
VccADAC	3.3V	0.0691A
VccFDIPLL	1.1V	VccVRM
VccACIK	1.1V	0.034A

LAN REALTEK RTL8111DL		
VDD33	3.3V	0.058A
EVDD12&DVDD12	1.2V	0.289A

SUPER I/O IT8720F-CX		
5VSB	5V	15mA
VCC	5V	60mA
BAT 3.3V	3.3V	2uA

AUDIO RTL662-VC2/888S-VC2		
DVDD 3.3V	3.3V	40mA
AVDD	5V	51mA

PCI Slot (per slot)		X1 PCIe per		X16 PCIe per	
5V	5.0A	3.3V	3.0A	3.3V	3.0A
3.3V	7.6A	12V	0.5A	12V	5.5A
12V	0.5A	3.3Vaux	0.375A	3.3Vaux	0.375A
3.3Vaux	0.375A				
-12V	0.1A				

USB X10 FR	USB X4 IO	2XPS/2
VDD 5VDual 2.0A	VDD 5VDual 2.0A	5VDual 1.0A

